電機メーカーにおける研究開発
－企業研究者の体験談－

（株）日立製作所　技師長

内山邦男

会社概要

2012年 (H24年)3月期

日立製作所

設　立	1920年2月1日(大正9年) [創業1910年]
本　社	東京都千代田区丸の内一丁目6番6号
資本金	4,277億円
売上高	1兆8,704億円
従業員数	3万2900人

日立グループ [連結]

売上高	9兆6,658億円
研究開発費	4,125億円 (対売上高 4.3%)
連結子会社数	939社 (国内: 340社、国外: 599社)
従業員数	32万3500人 (国内: 21万2300人、国外: 11万1200人)

コーポレート研究所

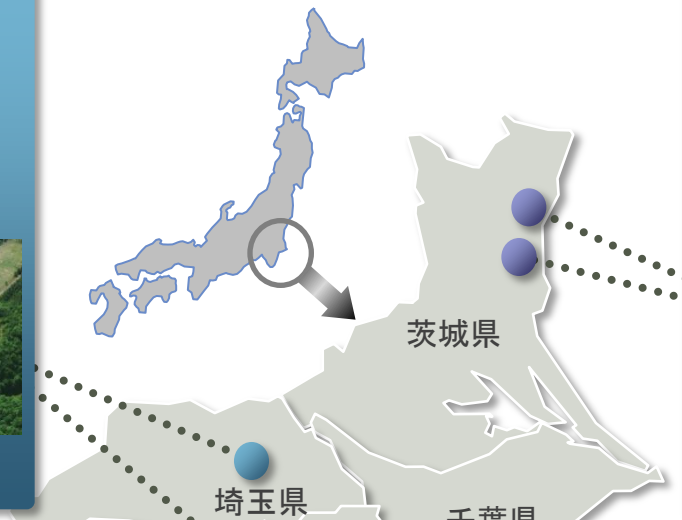
●2011年4月～

中央研究所
［ 約900名 ］

- グリーンICT
- エレクトロニクス
- ライフサイエンス・計測


東京都国分寺市


埼玉県鳩山町



日立研究所
［ 約1,200名 ］

- 次世代電池
- 材料
- 情報制御
- 機械
- エネルギー・環境


茨城県日立市


茨城県ひたちなか市

デザイン本部
［ 約150名 ］


東京都港区赤坂

横浜研究所
［ 約1,100名 ］

- 生産技術
- 情報サービス
- 情報プラットフォーム
- 映像情報


神奈川県横浜市

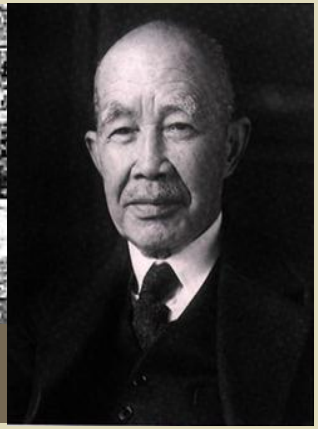
中央研究所　設立とその理念

設　立　　1942年4月(昭和17年)

理　念　　10年、20年後を目標とする基礎的研究を行なうとともに、今日の課題にも取り組む

馬場 粂夫　初代所長

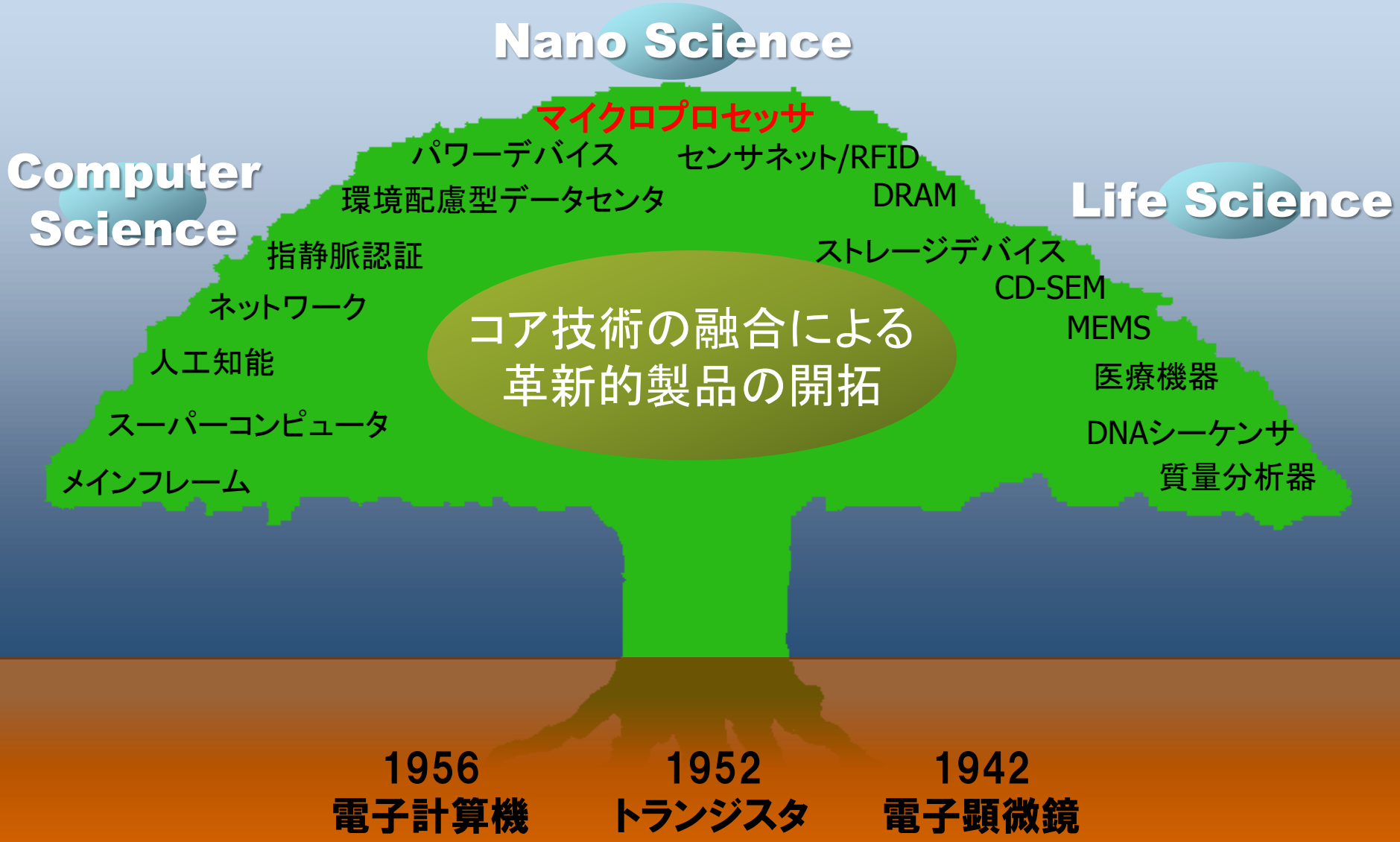
設立当時

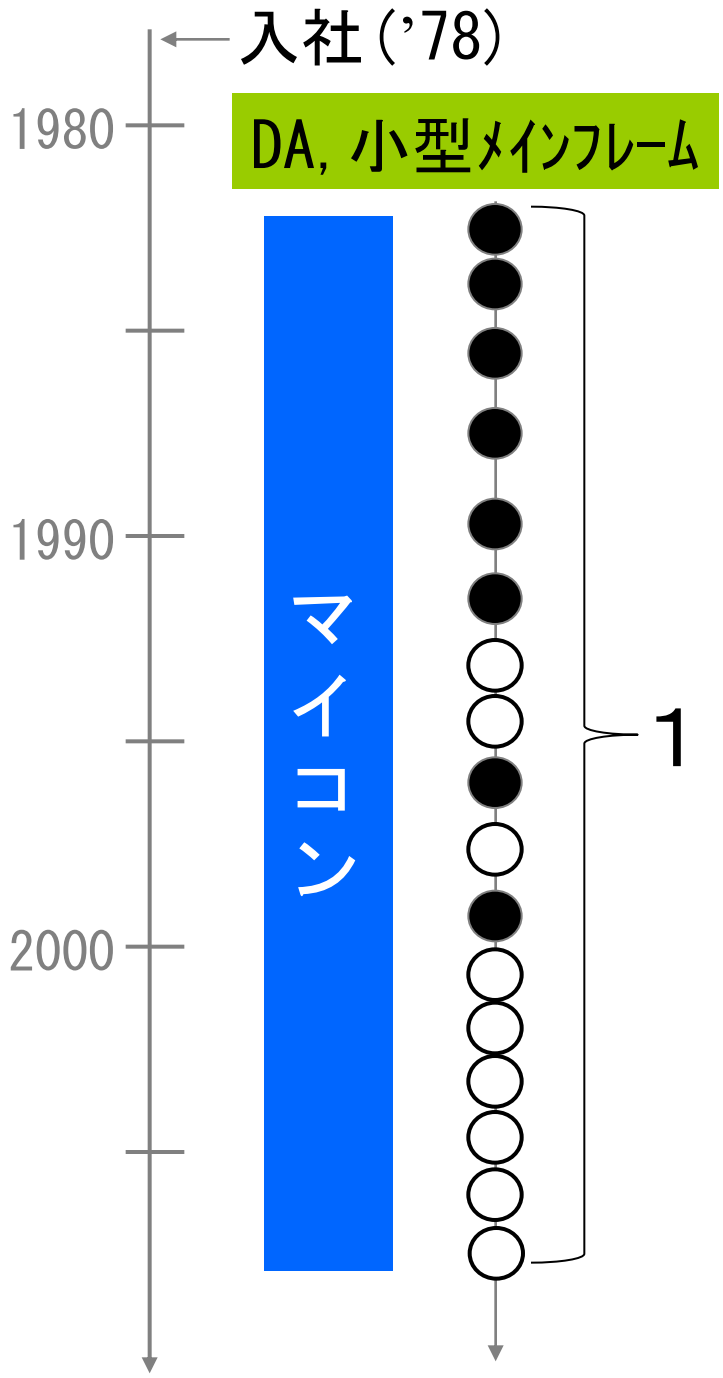


小平 浪平　創業社長

中央研究所　技術の樹

人と地球を支える21世紀型エレクトロニクス研究の加速





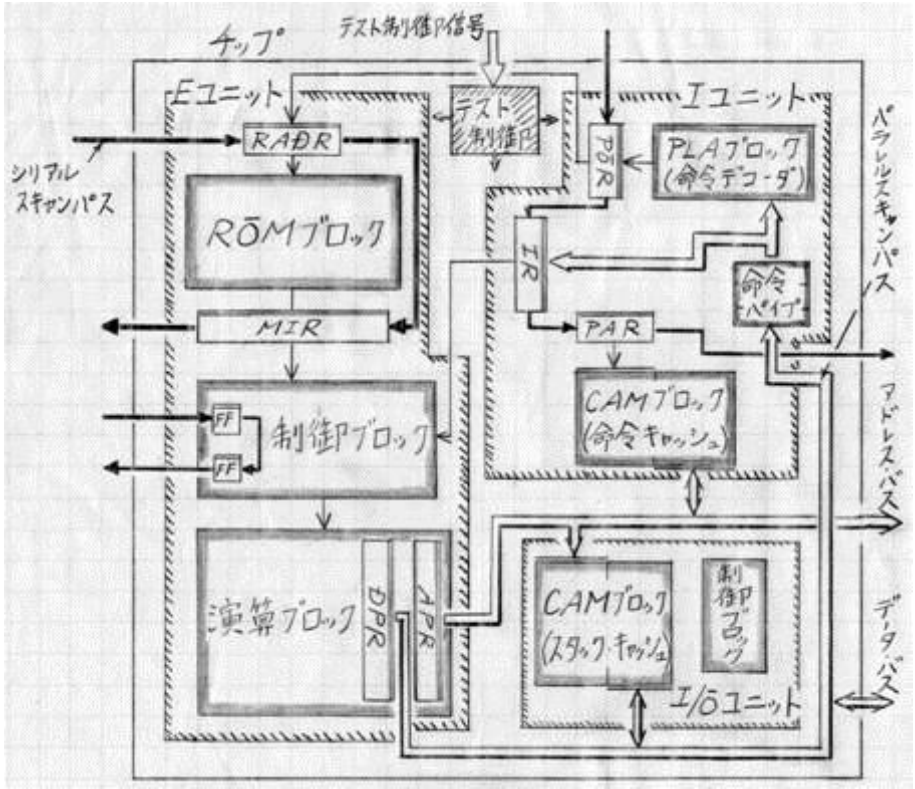
１７種のマイコンを開発

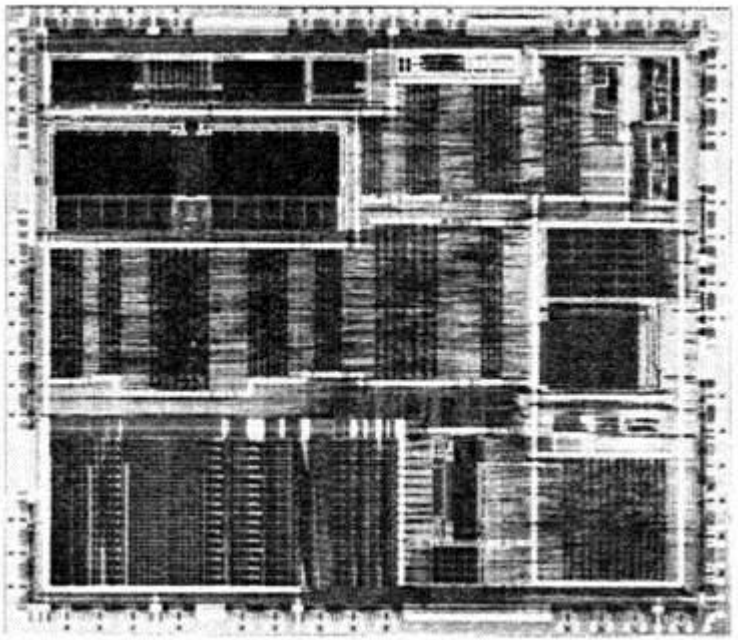
Mチップ (81～82)

- 小型メインフレームを1チップ化、2um CMOS
- 初めてのマイクロプロセッサ設計
- いきなり設計リーダ
  内山＋新人＋（設計外注）x2人
- 設計ファイル完成したが、論理シミュレーションまで至らず中止

MICRO32 （83～85）

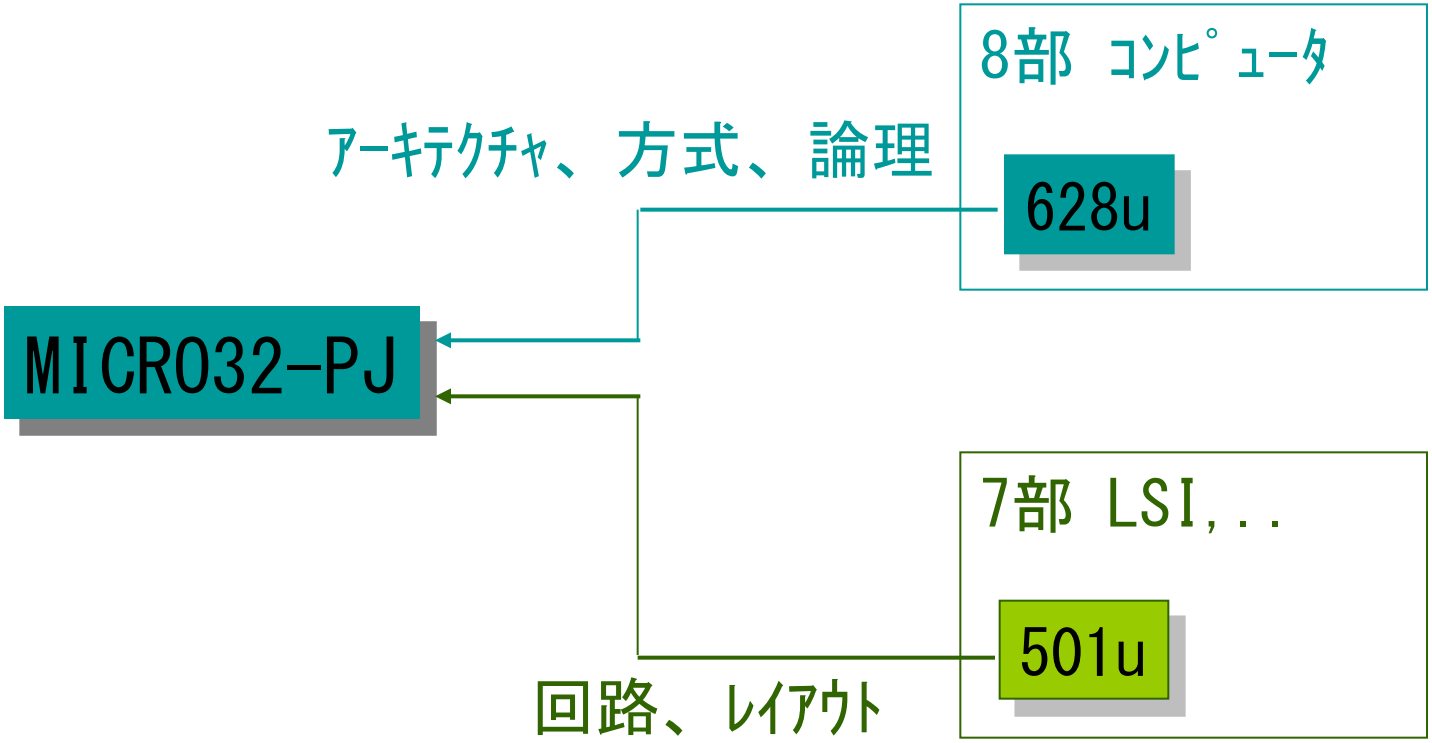
- 日立初の32ビットマイコン（世界でも先頭グループ）
- 1.3um CMOS, Al2, 391KTrs, 20MHz, 5MIPS
- 中央研究所LSIラインで試作





MICRO32 （83～85）

MICRO32-PJ: 専門分野の違うグループによるPJ体制

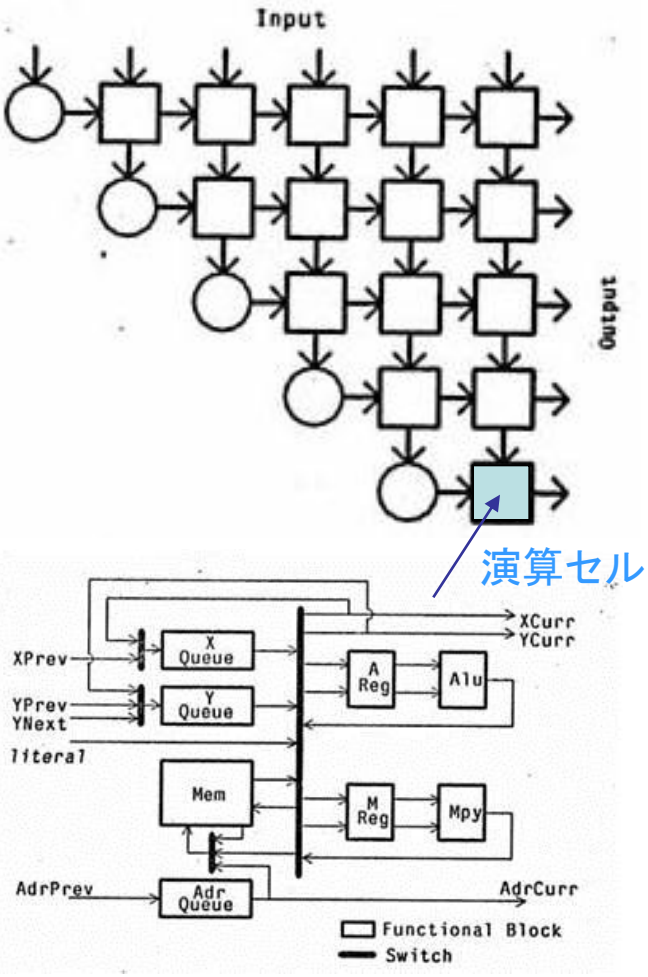


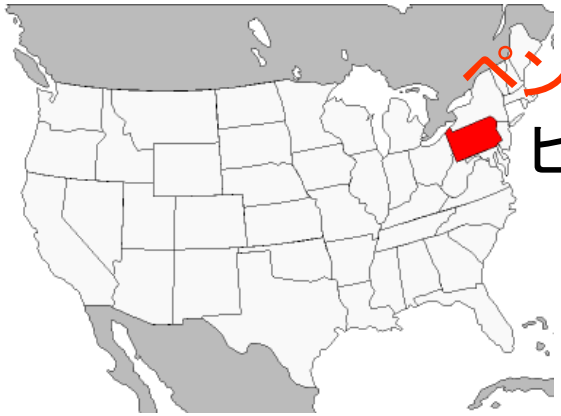
- 論理方式、回路にまたがる特許を創出（1983）
  ⇒ 日立マイコン事業を救う特許に

シストリックアレイ （85～86）

- 米国ｶｰﾈｷﾞｰﾒﾛﾝ大学に社費留学（１年間）

シストリックアレイ

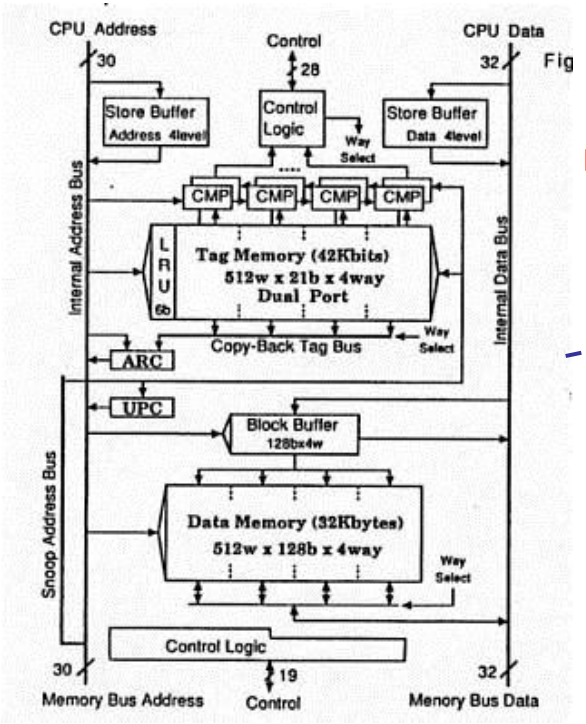




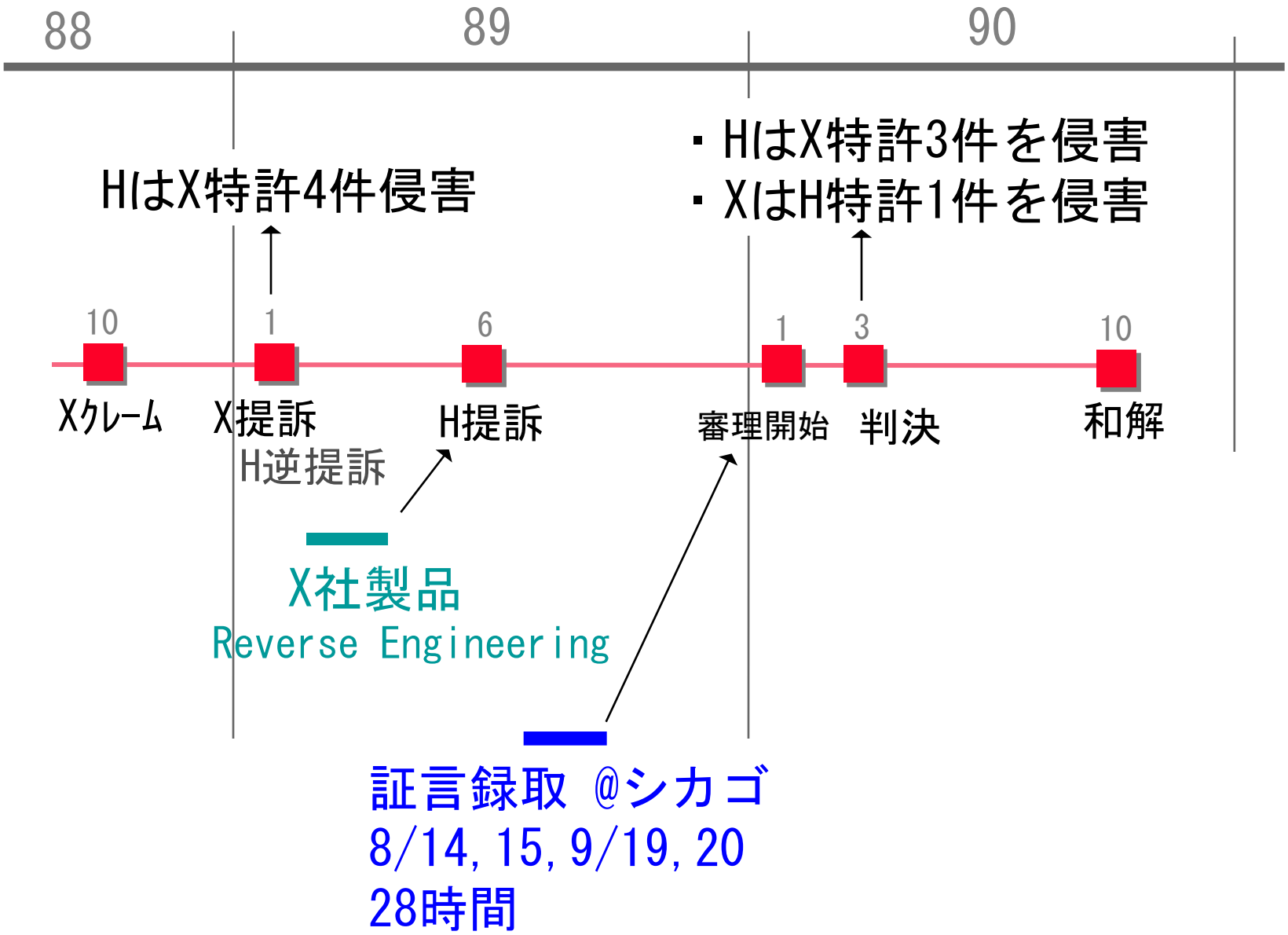
ｶｰﾈｷﾞｰﾒﾛﾝ大

キャッシュチップ （87～89）

- 事業部のメモリ設計Grと共同開発
- 全米をキャラバン（1988/5, 2週間）
  Apple, SUN, Sequent, Compaq, IBM, Wang, DEC, DG,...
- 製品化に至らず
- 初めて国際会議（VLSI symp.1990@Hawai)で発表



特許訴訟



明細書

Content Addressable Memory Having Dual Access Modes

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CONTENT ADDRESSABLE MEMORY HAVING DUAL ACCESS MODES

BACKGROUND OF THE INVENTION

This invention relates to a content addressable memory (hereinafter called "CAM").

CAM is a memory of the type which is addressable in accordance with the content for which coincidence is desired. This CAM is effective when retrieving a plurality of data in parallel with one another. The possible application of CAM in the field of computers may be an address array of cache memories, translation look-aside buffers for address conversion and various other applications. However, CAM has not yet been employed widely because the cost of CAM per bit is higher than that of a random access memory (hereinafter called "RAM"). It is expected, however, that CAM will gain a wide range application in future with further improvement in the integration density of LSI.

FIG. 1 shows a conventional content addressable memory device using CAM. Reference numerals 100 and 120 represent the array portions of CAM and RAM, respectively. Each word of CAMs 110a–110n stores the key to be retrieved. Each word of RAMs 120a–120n stores the data corresponding to each key stored in CAM. Each word of CAM is directly connected to that of RAM by signal line 130a–130n. This signal line is a word coincidence line when viewed from the CAM side, and is a word selection line when viewed from the RAM side. When the key to be retrieved is input by the signal line 140, it is compared in parallel with the key stored in each word of CAM, and the word coincidence line of the word which proves to be coincident is asserted. Therefore, the word selection line of the corresponding RAM is asserted, and the data belonging to the coincident key is read out from the RAM through the signal line 150. An example of a cache memory using such a content addressable memory device is disclosed, for example, in Japanese Patent Laid-Open No. 64,287/1982.

The first problem with a memory device of the kind described above is that the key and the data can not be stored simultaneously in the CAM and RAM. The key is temporarily stored in the CAM word, then, the RAM word selection line is selected by inputting the same key to the signal line 140; then, the data must be written into the RAM word through the signal line 150. The second problem is that an arbitrary RAM word line can not be selected easily because the RAM word selection line is directly connected to the CAM word coincidence line. In other words, it has been necessary to store in advance a predetermined key in the corresponding CAM word, and then to input that key to the CAM, in order to select a particular RAM word line.

SUMMARY OF THE INVENTION

The present invention is therefore directed to provide a content addressable memory device which eliminates the problems of the prior art devices described above, requires only a limited increase in hardware and yet has a regular structure suitable for fabrication in the VLSI arrangement.

In order to solve the problems of the prior art devices described above, the present invention disposes a selector between each word coincidence line on the CAM side and each word selection line on the RAM side, one of the inputs of the selector is used as the CAM word

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coincidence line and the other is used as the CAM word selection line with the selector output being connected to the RAM word selection line. According to this structure, the memory device can be used while utilizing fully the content addressable memory by selecting the selector input word coincidence line, and the memory device can be used as a whole as a RAM by selecting the selector input word selection line.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows the structure of a prior art device.

FIG. 2 shows the overall structure of one content addressable memory device in accordance with one embodiment of the present invention.

FIG. 3 is a circuit diagram of a CAM cell; and

FIG. 4 is a circuit diagram of an RAM cell.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, one embodiment of the present invention will be described in detail with reference to the accompanying drawings. FIG. 2 shows the overall structure of the content addressable memory device. This device has a CAM array 210 and an RAM array 220. The CAM array has an n bit by m-word construction, and each bit consists of one CAM cell 230. Each word of the CAM array consists of l CAM cells 230, and each cell is connected in the word unit to a word selection line 250 (W_0–W_m) on the CAM side and to a word coincidence line 260. A load MOS transistor 300 is connected to one of the ends of each word coincidence line 260, and the other side of the MOS transistor 300 is connected to a power source (V_{cc}). Each cell 230 of the CAM array 210 (hereinafter called "CAM cell") is connected in each bit to a data line A_0, $\overline{A_0}$–A_l, $\overline{A_l}$). The data line of each bit consists of two lines having opposite polarities.

The RAM array 220 has m-bit by n-word construction, and each bit consists of one cell 240 (hereinafter called "RAM cell"). Each word of the RAM array 220 consists of m RAM cells 240, and each cell is connected in the word unit to a word selection line (X_0–X_n) on the RAM side. Each RAM cell 240 of the RAM array 220 is connected in the bit line unit to a data line (D_0, $\overline{D_0}$–D_m, $\overline{D_m}$). The data line of each bit consists of two lines having opposite polarities with each other.

A selector 280 having two-input and n-bit construction is interposed between the CAM array 210 and the RAM array 220. N selectors 280 are disposed so as to correspond to the number of the words of the CAM array 210 and RAM array 220. One of the inputs of the selector 280 is connected to the word coincidence line 260 of the CAM array 210, and the other input is connected to the word selection line 250 on the CAM side.

The output of the selector 280 is connected to the word selection line 270 on the RAM side. Input selection of the selector 280 is controlled by a selector control line (hereinafter called "SC") 290. In other words, when SC 290 is asserted, the word coincidence line 260 is selected, and when SC 290 is negated, the word selection line 250 on the CAM side is selected.

The structure of the device described above is so regular that it can be easily accomplished with LSIs.

FIGS. 3 and 4 show the examples of the circuits of CAM cell 230 and RAM cell 240, respectively. MOS transistors T_1–T_4 in FIG. 3 and MOS transistors T_{11}–T_{16} in FIG. 4 constitute static flip-flops, respectively, each storing one-bit data. When the word selection line (WI) 250 on the CAM side or the word selection line (XI) 270 on the RAM side is asserted, the MOS transistors T_5, T_{10} or T_{15}, T_{16} are turned on, the data is read out from the data line (AI, $\overline{AI}$) 310 or the data line (Dk, $\overline{Dk}$) 320. In order to write the data, the word selection line is asserted, and the data is applied to the data line.

The CAM cell 230 shown in FIG. 3 has the function of judging whether or not the data stored in the flip-flops T_1–T_4 are coincident with the data on the data line 310. The MOS transistors T_5–T_8 bear that function. When the data are not coincident, both of the MOS transistors T_7 and T_8 are turned on or both of the MOS transistors T_5 and T_6 are turned on, and the word coincidence line 260 is grounded. Since the word line 260 is connected to all the bits of the CAM cell 230 constituting the word as shown in FIG. 1, when the l-bit data that are applied to the data line 310 and the data stored in the word of the CAM array 210 are not coincident with each other, the corresponding word coincidence line 260 is grounded, that is, the line is negated. When they are coincident, on the other hand, it has a high voltage level and is brought into the asserted state. In this manner, the content of each word is retrieved by applying the data to the data line 310 of the CAM array 210, and the word coincidence line 260 corresponding to the coincident word is asserted.

The content addressable memory device shown in FIG. 2 has substantially two modes. In one of the modes, the associative function of the CAM array 210 is utilized fully, and the access is made to the RAM array 220 in accordance with the result of association. This is realized by asserting SC 290. Under this state, the word coincidence line 260 of each word of the CAM and RAM arrays 210, 220 is connected to the word selection line 240 on the RAM side, as described earlier. When the data is applied to the data line 310 on the CAM side, therefore, the word coincidence line 260 corresponding to the word of the CAM array 210, in which the content which is coincident with that data is stored, is asserted, and the word selection line 270 of the corresponding RAM array 220 is further asserted, so that the data stored in that word is read out on the data line 320 on the RAM side. If the data is applied to the data line 320 on the RAM side under this state, the data is written into the selected word.

The other mode of the content addressable memory device is the mode in which the device is used as a whole in the same way as an ordinary RAM array. This is realized by negating SC 290. Under this state, the word selection line 250 on the CAM side of each word of the CAM and RAM arrays 210, 220 is connected to the word selection line 270 on the RAM side via the selector 280. Therefore, an RAM array having a $(l+m)$ bit by n-word construction is constituted as a whole. When the word selection line 250 on the CAM side is

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asserted, the corresponding word selection line 270 on the RAM side is also asserted, and the word selection lines of the $(l+m)$ bit cells are asserted as a whole. Accordingly, read-out/write-in corresponding to the same word of the CAM and RAM arrays can be made simultaneously.

Since the content addressable memory device in accordance with the present invention has a regular construction, it is suitable for VLSI, and the chip area can be utilized effectively because an unnecessary wiring area is not necessary.

As can be seen from the above description, it is possible to address the RAM array in accordance with the result of association of the CAM array, and to access the whole device as the RAM array.

Therefore, the operation of storing the key in the CAM word and the operation of writing the data in the RAM word can be made simultaneously.

Furthermore, an arbitrary word RAM line can be easily selected, and the data writing operation to the RAM can be simplified.

As described above, the present invention can provide a content addressable memory device having extremely high versatility and a wide range of application.

What is claimed is:

1. A content addressable memory device comprising:

a content addressable memory array having word coincidence lines, word selection lines and data lines;

a random access memory array having word selection lines and data lines; and

means responsive to a control signal for selecting either the word coincidence lines or the word selection lines of said content addressable memory array and for connecting the selected lines to the word selection lines of said random access memory array.

2. The content addressable memory device as defined in claim 1 wherein said content addressable memory array consists of a plurality of cells, each cell being connected to a word selection line, a word coincidence line and a data line, and including means for storing data received on the data line when the word selection line is selected and means for comparing the data on said data line with the stored data of said storing means and for changing the potential level of the word coincidence line on the basis of the result of comparison.

3. The content addressable memory device as defined in claim 2 wherein said storing means in each cell consists of a flip-flop.

4. The content addressable memory device as defined in claim 1 wherein the number of the data lines of said content addressable memory array is different from the number of the data lines of said random access memory array.

FIG. 3

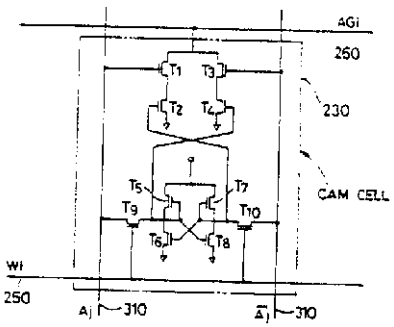
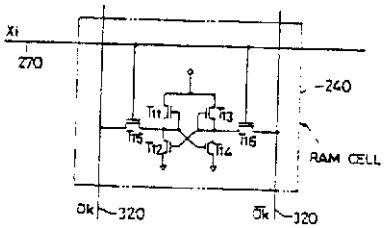
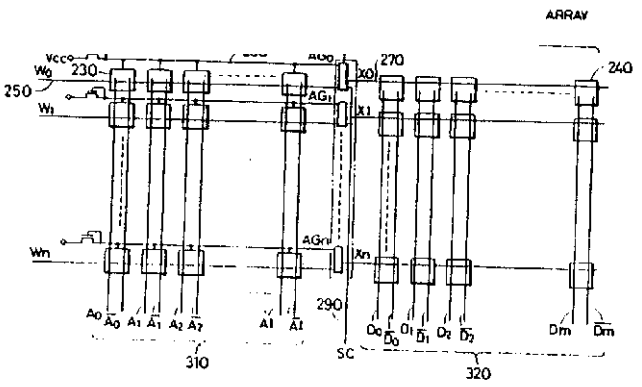
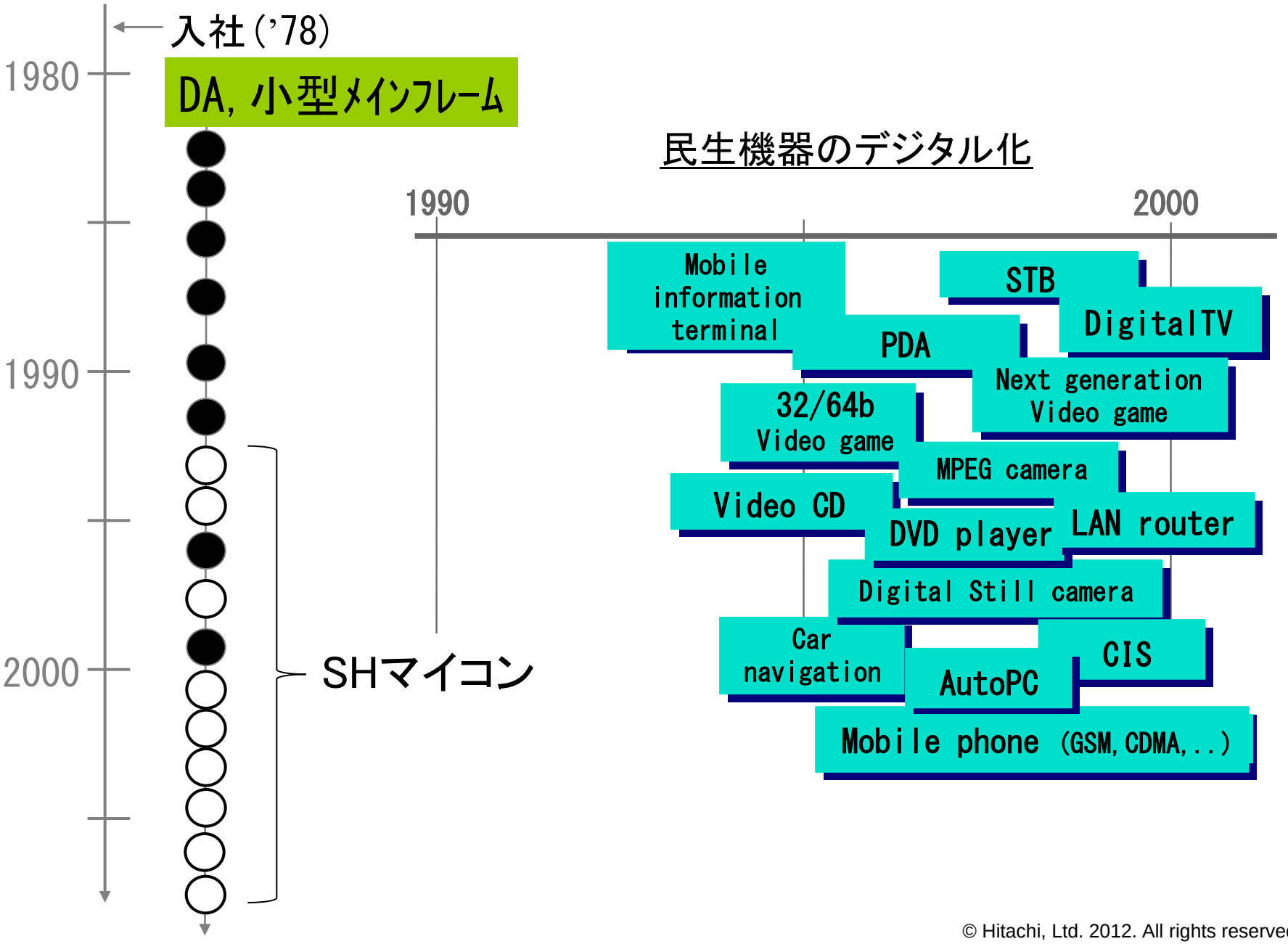


FIG. 4

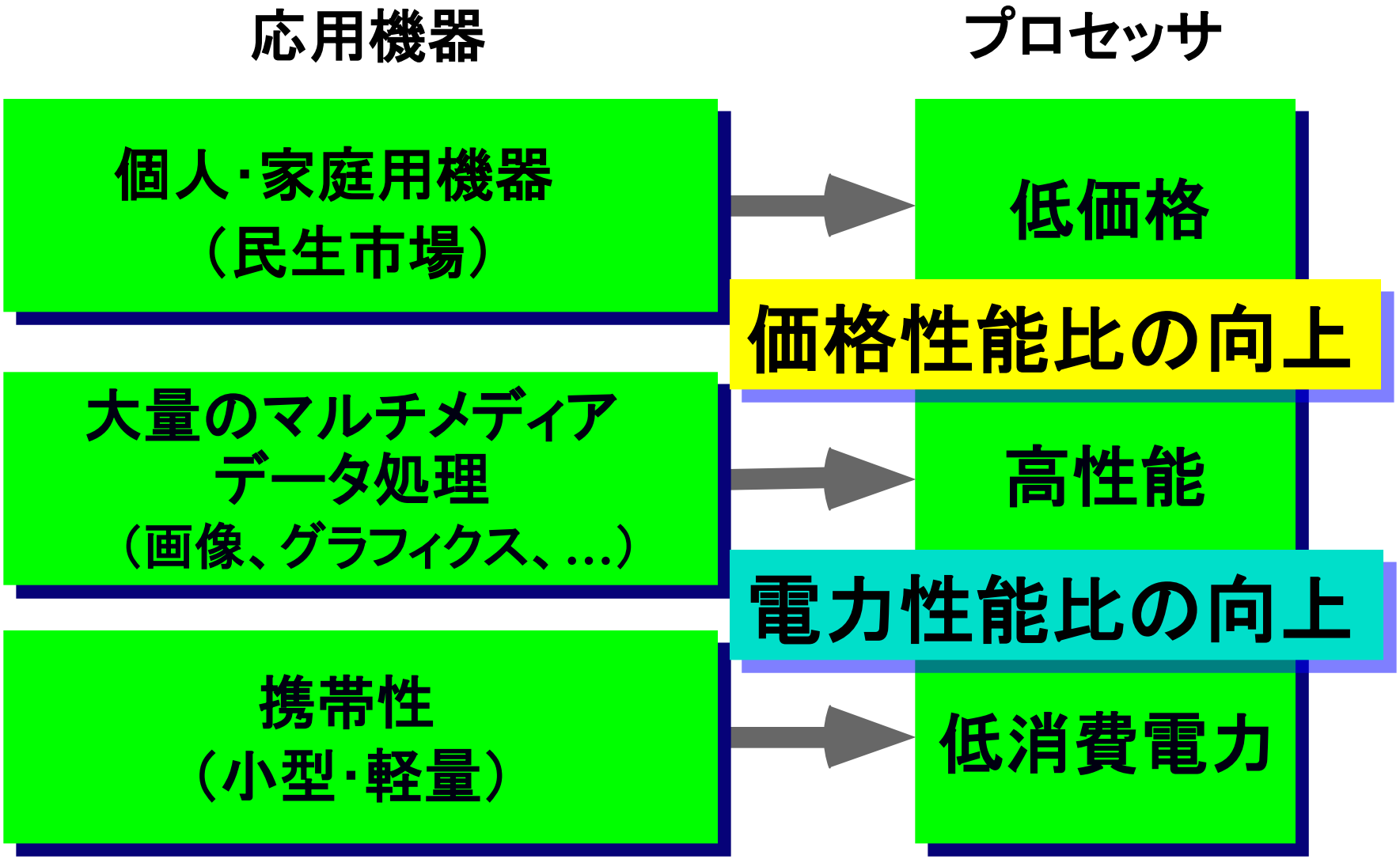




SHマイコン

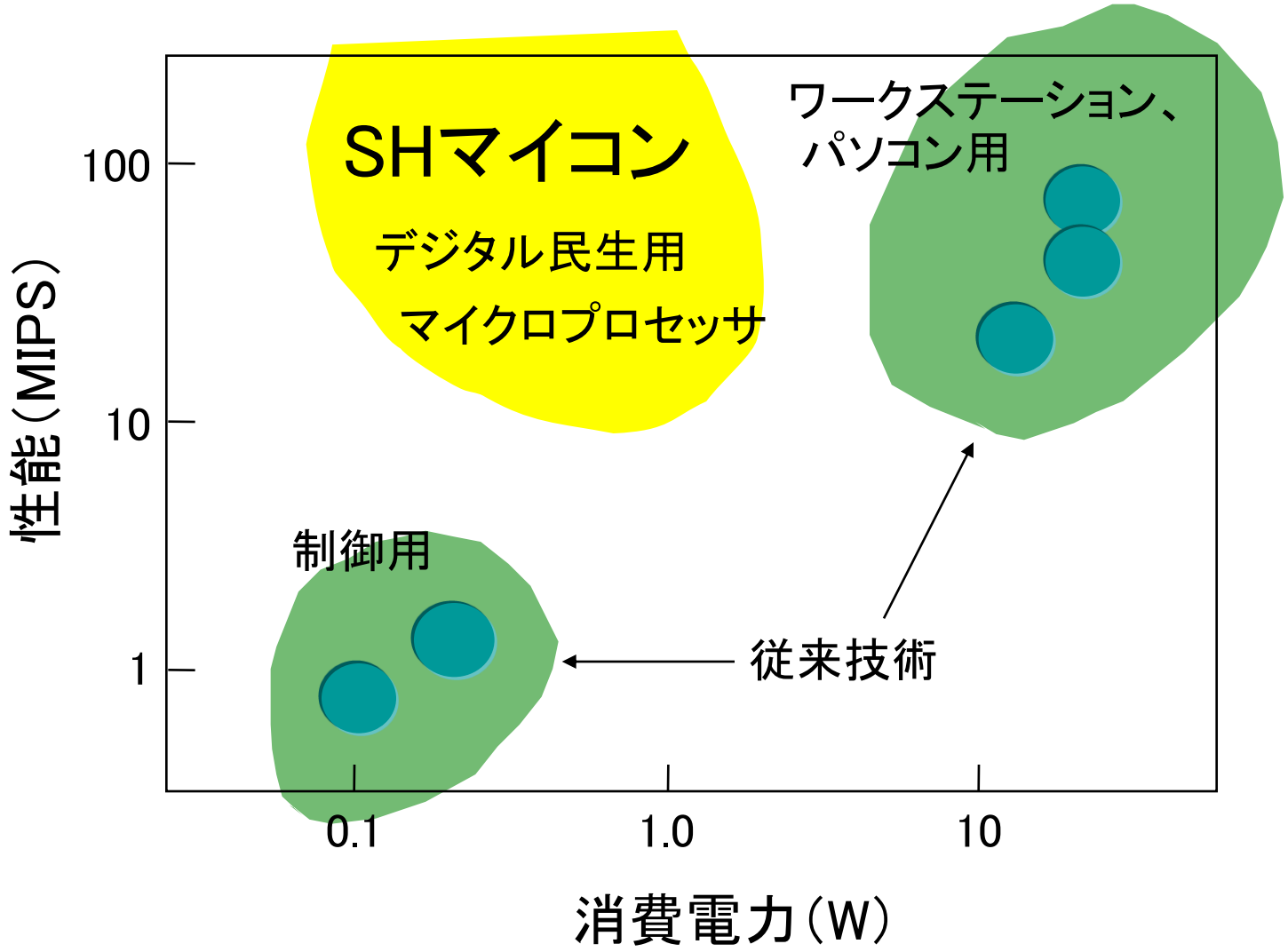


マイクロプロセッサに対する新しいニーズ

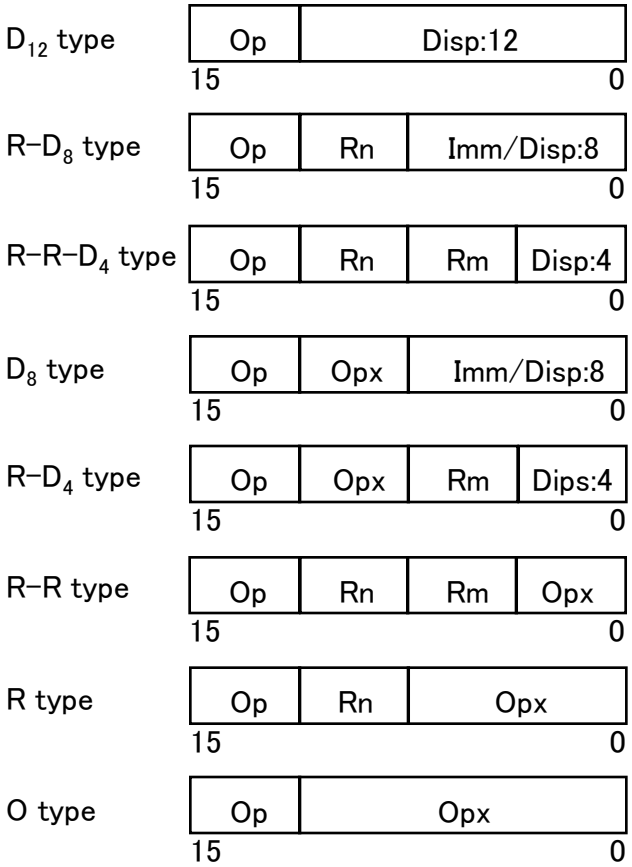


SHマイコンの狙い

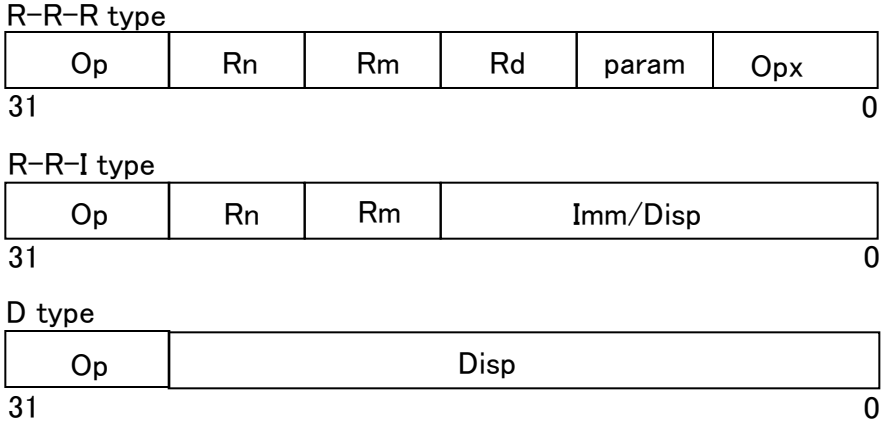
（1990年代初頭）



SHマイコンの命令フォーマット



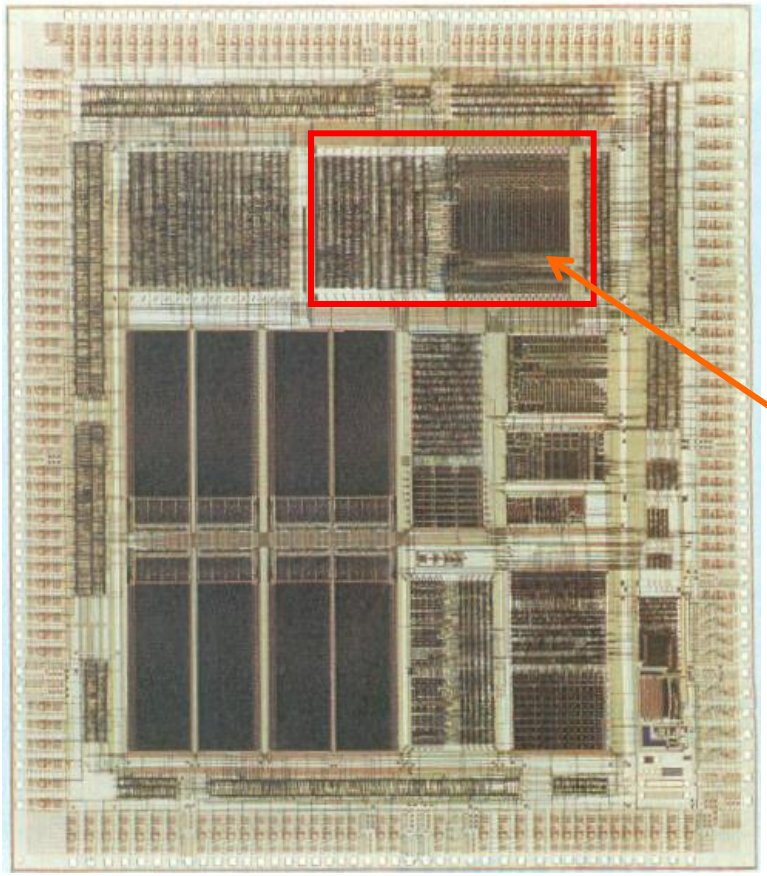
SHアーキテクチャ



従来型RISCアーキテクチャ

SH-1（’93）

- 0.8um, 20MHz, 16MIPS
- 狙った応用：HDD,VTR,FAX,PRT,PDA,...



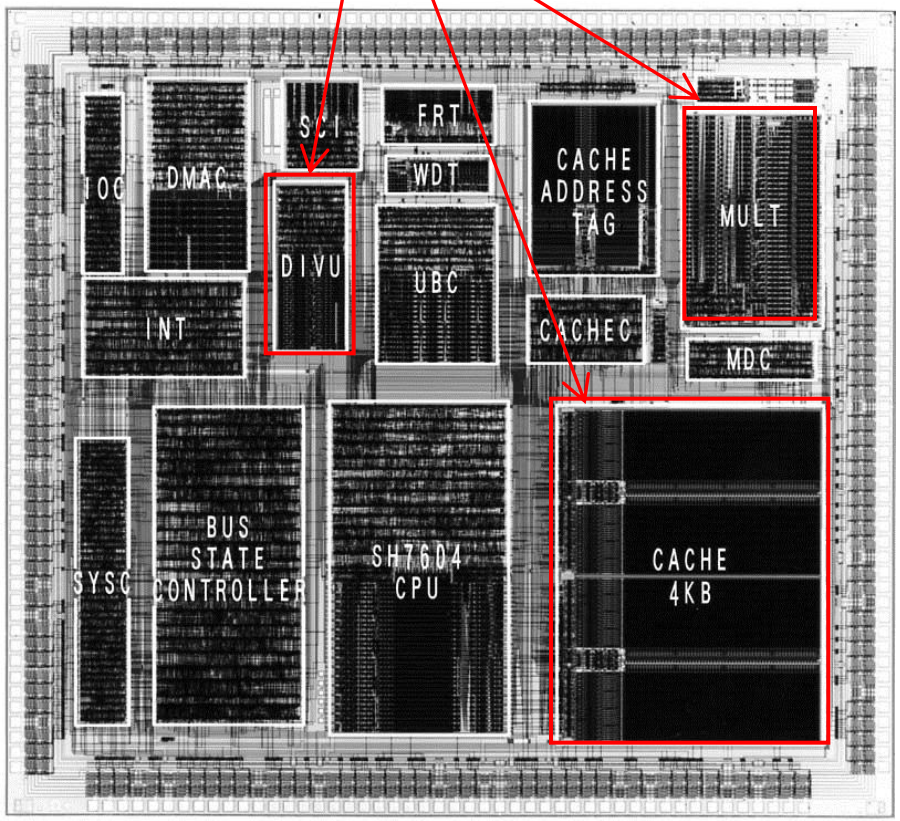
25万画素デジカメに搭載
世界初のデジカメヒット商品

CPUコア
8mm^2
2MIPS/mm^2

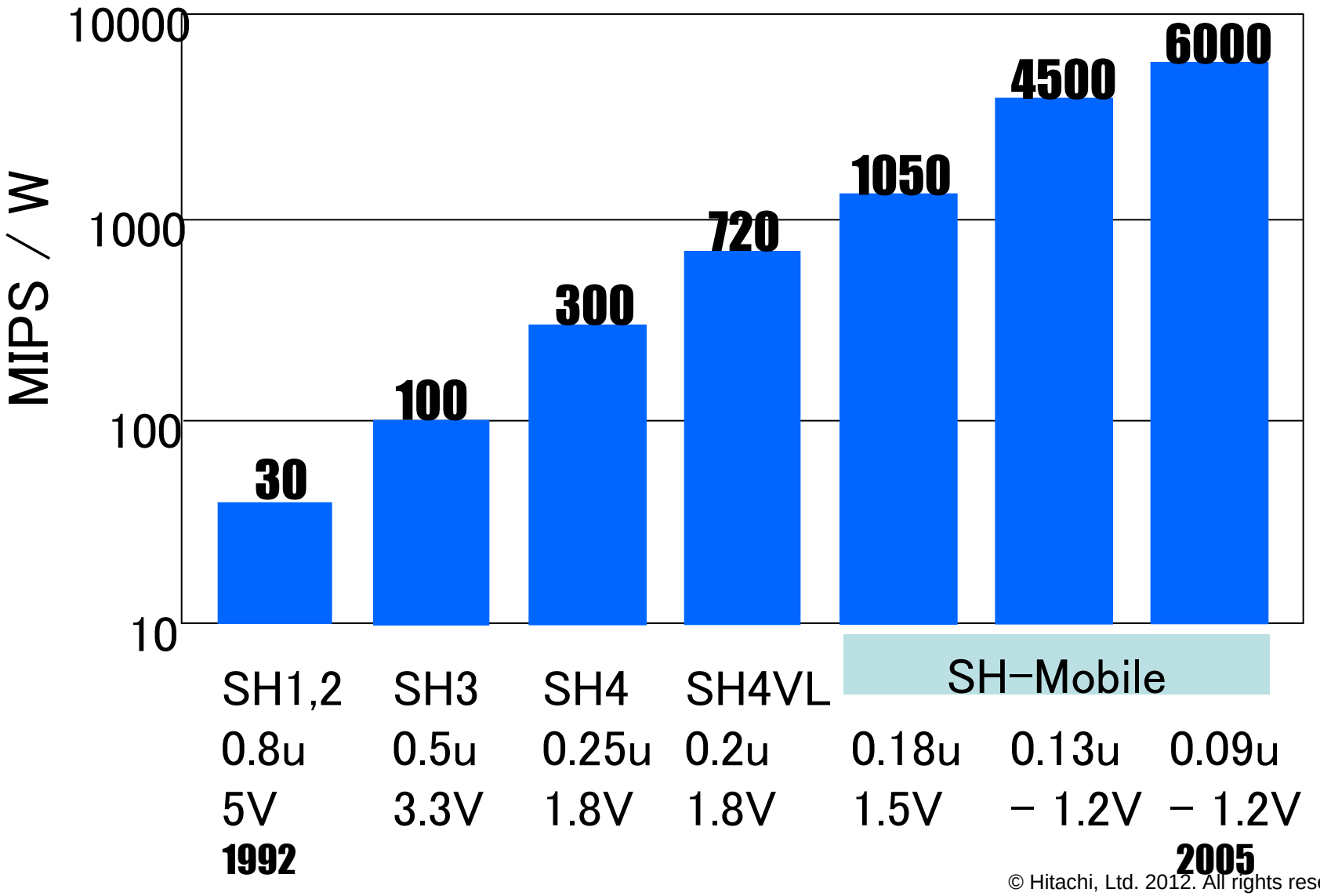
*1）当時のマイコン(H8/500)
0.1MIPS/mm^2

SH-2（’94）

- 0.8um, 28.7MHz, 25MIPS, 500mW
- 世界最高の電力性能比、世界シェアトップ
- ゲーム機向け機能強化

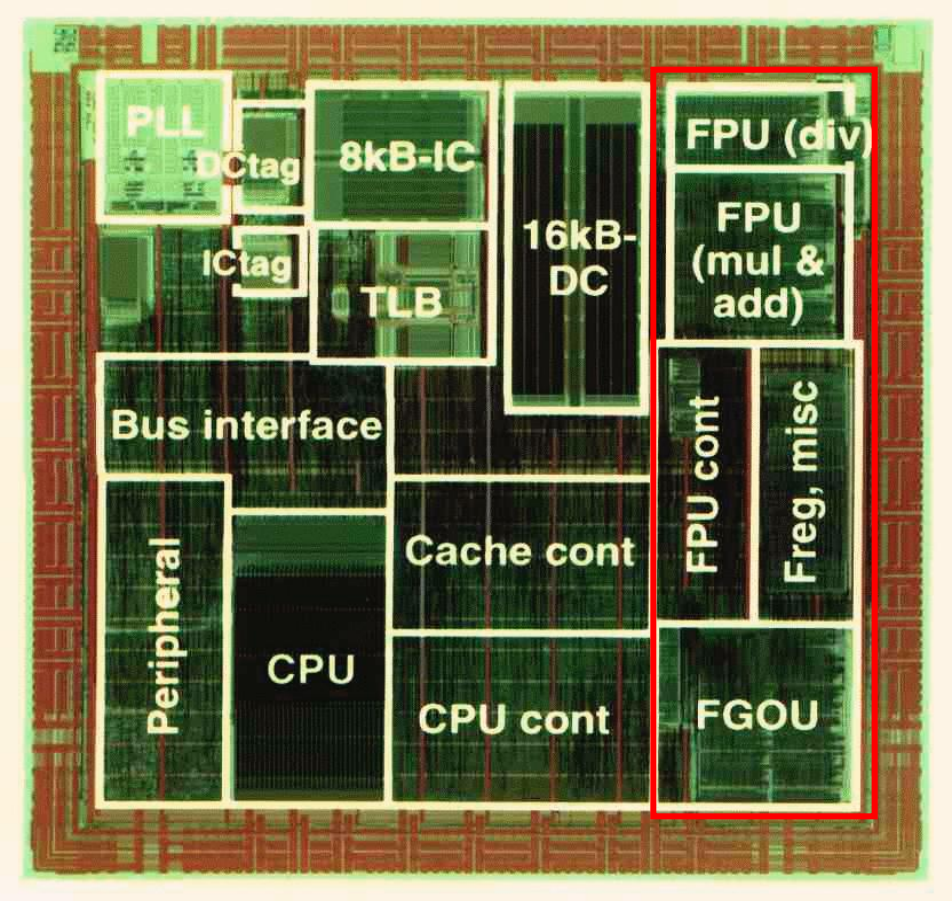


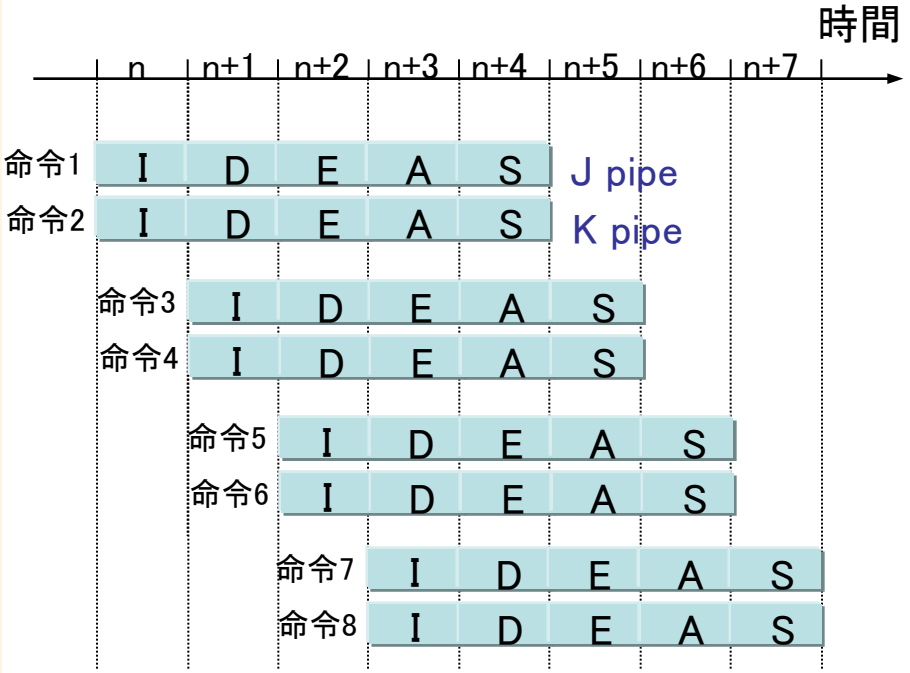
世界最高の電力性能比



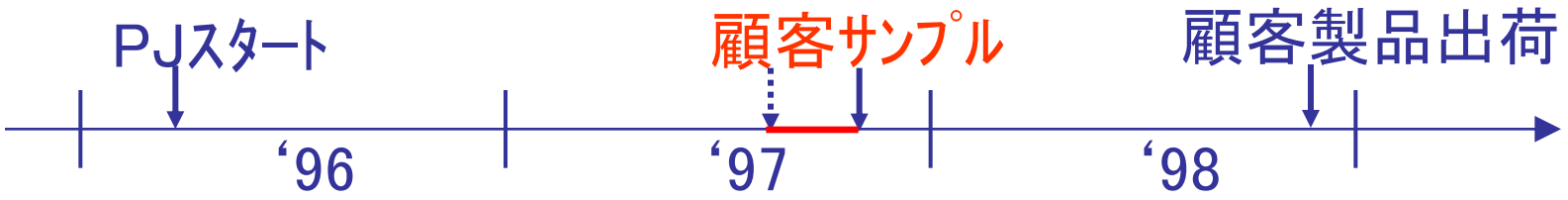
SH-4（’98）

- 0.25um, 200MHz, 360MIPS（SH3x6倍）, 1.2W
- ゲーム機向け、2-wayスーパースカラ、世界初3DG演算





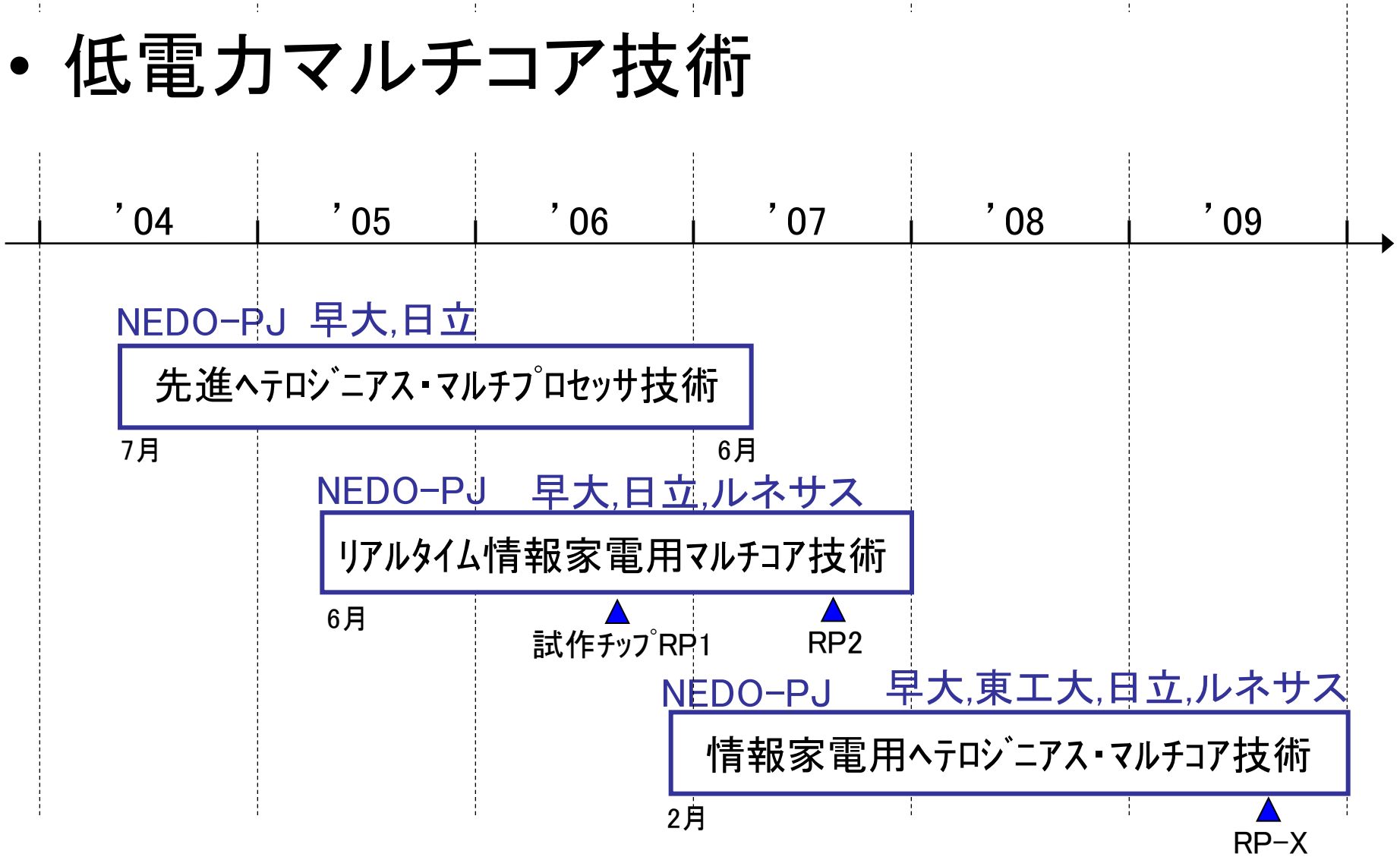
SH-4 （96～98）



- 96春からPJスタート，97夏に顧客サンプル
- 中央研究所に70名集結
- 海外リソース利用：米国（回路），インド（テストプログラム）
- 問題続出：論理バグ，回路不具合（クロック，キャッシュ）
- 0.25umプロセス不具合で3ヶ月良品取れず（97/8-11），3ヶ月毎朝レビュー（論理-回路-プロセス）
- ゲームソフト開発支援のため顧客に若手派遣
- 顧客ゲーム機は1100万台出荷して販売中止（’01/3）
  ＝＞SH-4技術をカーナビ、SH-Mobileに展開

オープンイノベーション（産学連携）

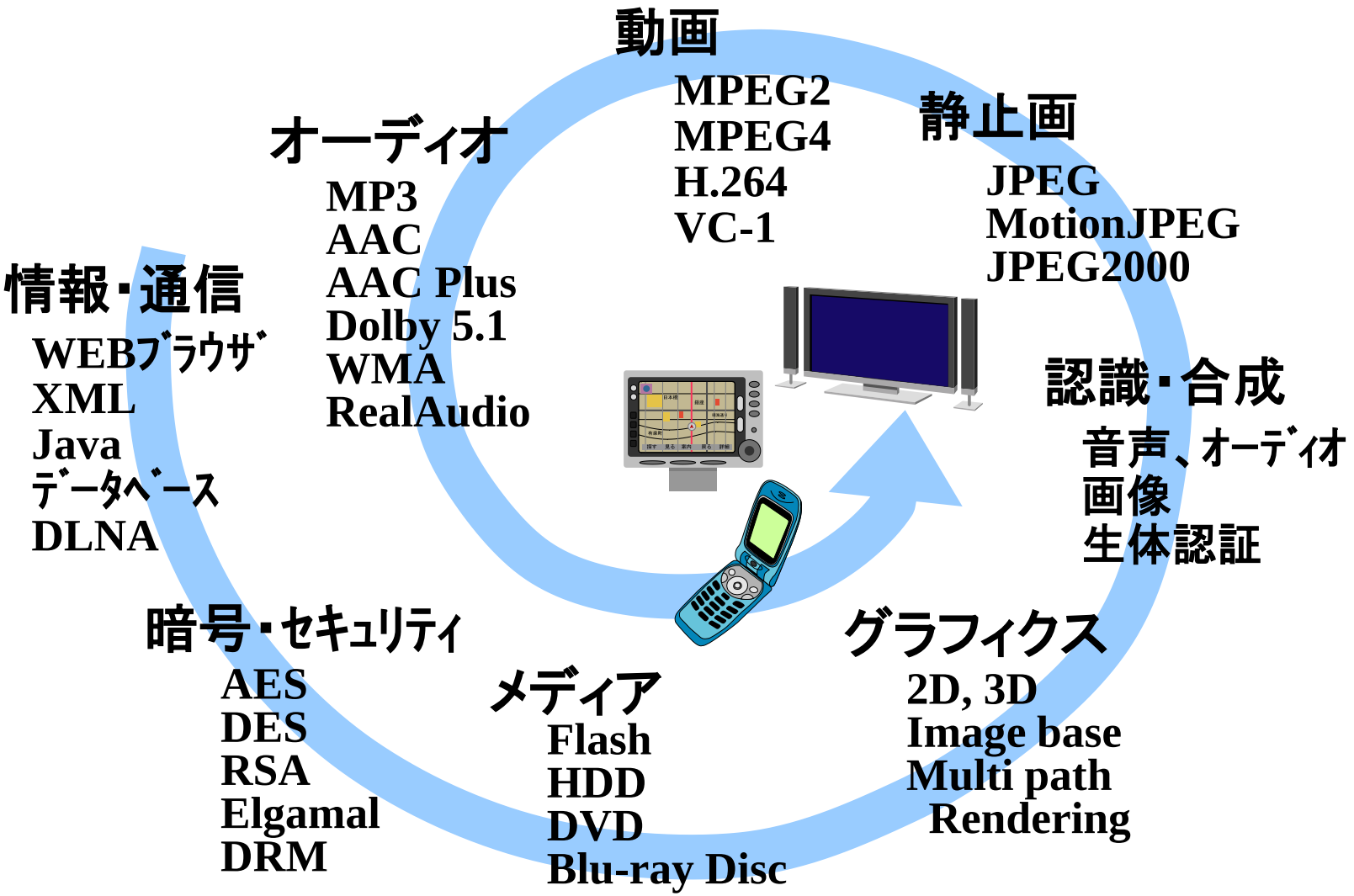
- 低電力マルチコア技術



デジタルコンバージェンス

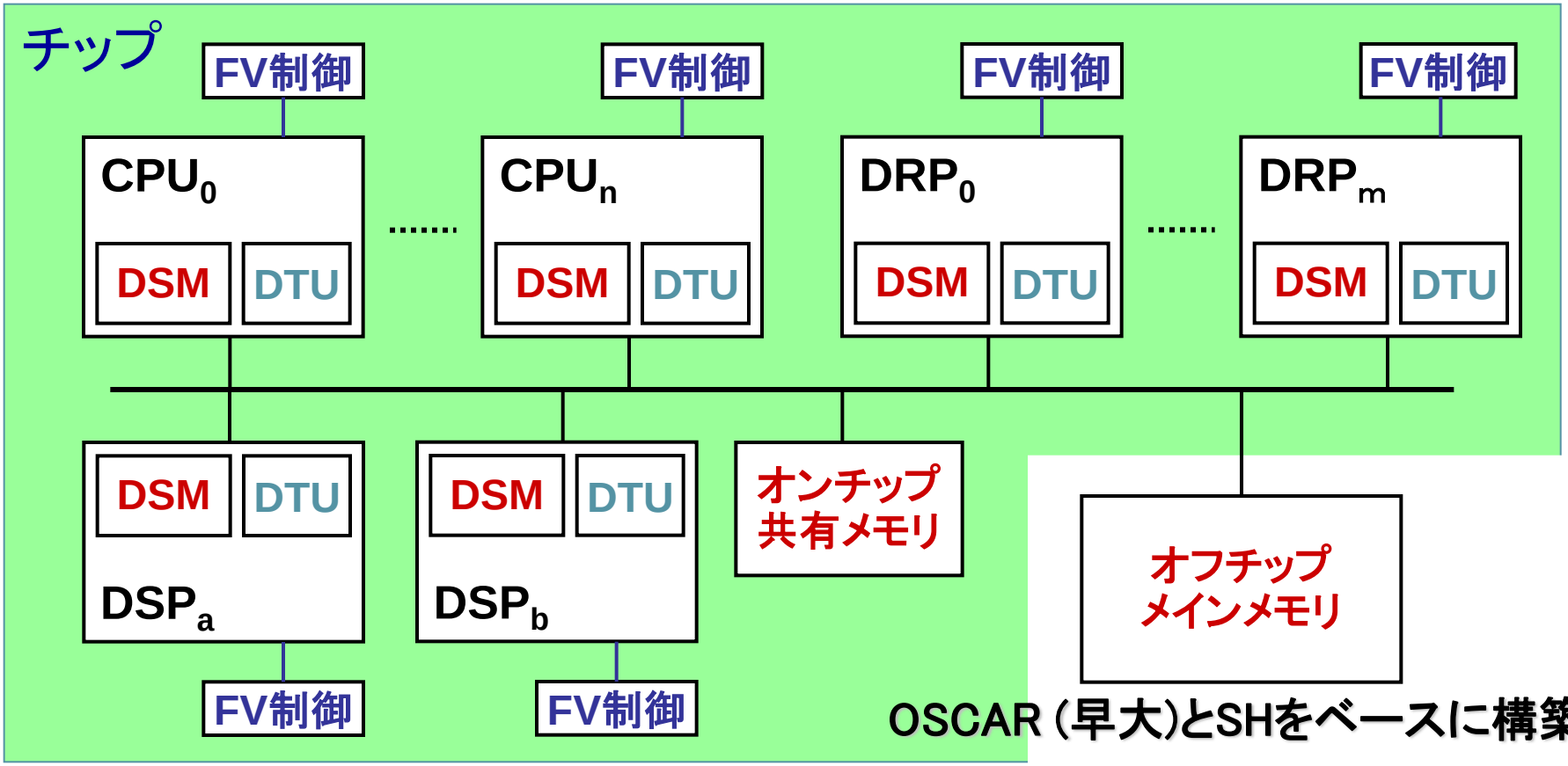
「Being Digital」’95, MIT

様々なデジタルアプリケーションが一つの機器に収斂



分散メモリ型マルチコア

- 複数の低電力な汎用プロセッサ、専用プロセッサをチップ上に搭載
- 各プロセッサは分散メモリ(DSM)、データ転送ユニット(DTU)を内蔵
- 各プロセッサは個別に周波数・電圧(FV)制御が可能

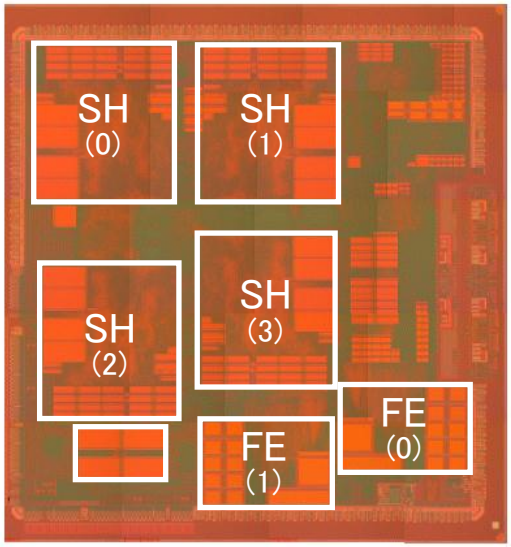


OSCAR (早大)とSHをベースに構築

DSP:信号処理プロセッサ、DRP:動的再構成プロセッサ

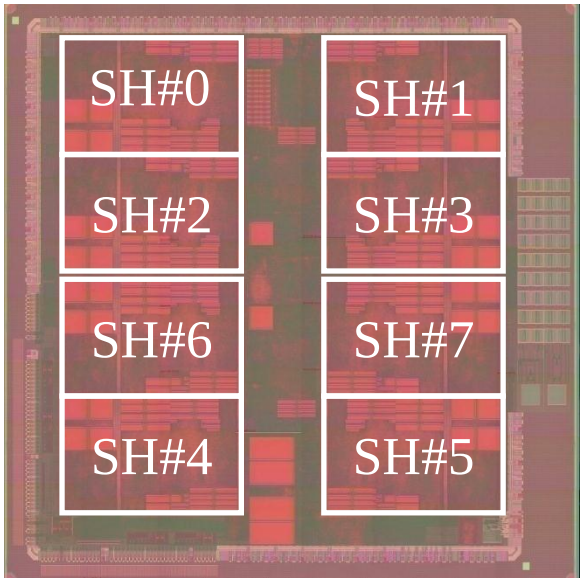
試作チップ

4xCPU搭載



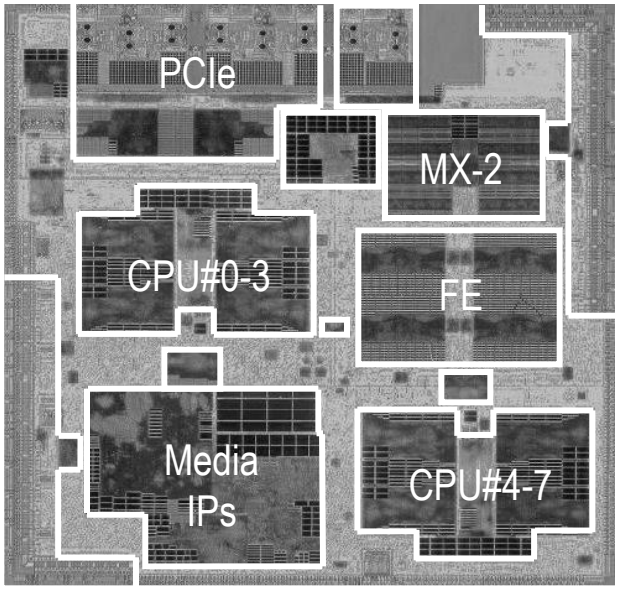
ISSCC2007で発表

8xCPU搭載



ISSCC2008で発表
LSI of the Year 2009受賞

8xCPU+4xFE+2xMX搭載



ISSCC2010,
COOL Chipsで発表

ISSCC（国際固体素子回路会議）会場　マリオット・ホテル（サンフランシスコ）

学会活動

- 電子情報通信研学会
  集積回路研究専門委員会、委員長
- Integrated Circuits and Devices in Vietnam, Chair
- IEEE SSCS Japan Chapter, Chair
- IEEE COOL Chips, Vice Chair
- ASP-DAC Designer’s Forum, Chair
- 他

Integrated Circuits and Devices in Vietnam (ICDV)

ICDV 2010

Location: Ho Chi Minh City University of Technology (HCMUT)

Date: August 16, 2010 (Monday) – August 18, 2010 (Wednesday)

最後に

- No.1技術を目指そう
  横と縦の理解を大切に
- 企業の研究では出口が必要
  一つの出口にこだわることはない
- 幅広い人脈を
  社内外、国内外