JEITA

Standard of Japan Electronics and Information Technology Industries Association

EIAJ ED-5005A

1.2V±0.1V (normal range) and 0.8V to 1.3V (wide range) power supply voltage and interface standard for non-terminated digital integrated circuits

Revised April, 2006

Investigated by

Technical Standardization Committee on Semiconductor Devices

Published by

Japan Electronics and Information Technology Industries Association

This document is a translation without guarantee. In the event of any doubt arising, the original standard in Japanese is to be evidenced.
JEITA standards are established independently to any existing patents on the products, materials or processes they cover. JEITA assumes absolutely no responsibility toward parties applying these standards or toward patent owners.
© 2006 by the Japan Electronics and Information Technology Industries Association All rights reserved. No part of this standard may be reproduced in any form or by any means without prior permission in writing from the publisher.

Contents

	•	page
For	reword ······	••••1
1.	Scope	1
2.	Standard specifications	1
2.1	Absolute maximum continuous ratings ······	1
	Recommended operating conditions	
2.3	DC specifications	2
2.4	Optional DC electrical characteristics for Schmitt trigger operation	2
3.	Test conditions	3
3.1	Positive Going Threshold Voltage ·····	3
3.2	Negative Going Threshold Voltage	3
Exi	planation ·····	5

Standard of Japan Electronics and Information Technology Industries Association

1.2V±0.1V (normal range) and 0.8V to 1.3V (wide range) power supply voltage and interface standard for non-terminated digital integrated circuits

Foreword To provide this standard of specification for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1. Scope This standard defines power supply voltage ranges, DC interface parameters for a family of non-terminated digital circuits operating from a power supply of 1.2V and driving/driven by parts of the same family, or mixed families which comply with the input/output interface specifications.

The specifications in this standard represent a minimum set or "base line" set of interfaces for CMOS-compatible circuits.

- **2. Standard specifications** All voltages listed are referenced to ground except where noted.
- **2.1 Absolute maximum continuous ratings** Absolute maximum continuous ratings give in table 1.

Table 1 Absolute maximum continuous ratings (1)

Parameter	Symbol	Test condition	Rating	Unit
Power supply voltage	$V_{ m DD}$	_	− 0.5 ~ 1.8	V
DC input voltage	V _{IN}	excluding I/O pins	$-0.5 \sim V_{DD} + 0.5 (\le 1.8 \text{ max})$	V
DC output voltage	V _{OUT}	including I/O pins	$-0.5 \sim V_{DD} + 0.5 (\le 1.8 \text{ max})$	V
DC input current	I_{IN}	$V_{IN} < 0V$ or $V_{IN} > V_{DD}$	±20	mA
DC output current	I_{OUT}	$V_{OUT} < 0V \text{ or } V_{OUT} > V_{DD}$	±20	mA
Storage temperature range	T_{STG}	_	(²)	°C

Note(1): Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum conditions is not implied, if it is beyond recommended operating conditions.

Note $\binom{2}{1}$: To be specified by manufacturers.

2.2 Recommended operating conditions

2.2.1 Normal range Normal range of recommended operating conditions give in table 2.

Table 2 Normal range of recommended operating conditions

Parameter	Symbol	Operating range	Unit
Power supply voltage	$V_{ m DD}$	1.1 ~ 1.3	V
Operating temperature range	T_a	(3)	°C

Note(³): To be specified by manufacturers.

2.2.2 Wide range Wide range of recommended operating conditions give in table 3.

Table 3 Wide range of recommended operating conditions

Parameter	Symbol	Operating range	Unit
Power supply voltage	V_{DD}	0.8 ~ 1.3	V
Operating temperature range	Ta	(⁴)	°C

Note(4): To be specified by manufacturers.

- **2.3 DC specifications** All voltages listed are referenced to ground except where noted.
- **2.3.1** Normal range Normal range of DC specifications give in table 4.

Table 4 Normal range of DC specifications(⁵)

Parameter	Symbol	Test condition	Min	Max	Unit
Power supply voltage	V_{DD}	-	1.1	1.3	V
High-level input voltage	V_{IH}	V _{OUT} ≥V _{OH} (min)	$0.65 V_{DD}$	V _{DD} +0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} (max)$	-0.3	$0.35V_{DD}$	V
High-level output voltage	V _{OH}	$I_{OH} = -2mA$	$0.75V_{DD}$	-	V
Low-level output voltage	V _{OL}	$I_{OL} = 2mA$	_	$0.25V_{DD}$	V

Note(5): V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.

2.3.2 Wide range Wide range of DC specifications give in table 5.

Table 5 Wide range of DC specifications(⁶)

Parameter	Symbol	Test condition	Min	Max	Unit
Power supply voltage	V_{DD}	-	0.8	1.3	V
High-level input voltage	V_{IH}	V _{OUT} ≥V _{OH} (min)	$0.7V_{DD}$	V _{DD} +0.3	V
Low-level input voltage	$V_{\rm IL}$	$V_{OUT} \leq V_{OL} (max)$	-0.3	$0.3V_{DD}$	V
High-level output voltage	V _{OH}	$I_{OH} = -100 \mu A$	V _{DD} -0.1	_	V
Low-level output voltage	V _{OL}	$I_{OL} = 100 \mu A$	_	0.1	V

Note(6): V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.

- **2.4 Optional DC electrical characteristics for Schmitt trigger operation** All specifications in the following tables apply across the operating temperature range.
- **2.4.1 Optional Schmitt trigger operation Normal range** Normal range of optional schmitt trigger operation give in table 6.

Table 6 Normal range of optional schmitt trigger operation (7)(8)

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{DD}	Supply Voltage	_	1.1	1.3	V
$V_t + (V_p)$	Positive Going Threshold Voltage	V _{OUT} ≥V _{OH} (min)	$0.4V_{\mathrm{DD}}$	$0.7V_{DD}$	V
V_{t} - (V_{n})	Negative Going Threshold Voltage	V _{OUT} ≤V _{OL} (max)	$0.3V_{DD}$	$0.6V_{DD}$	V
$V_h (V_t)$	Hysteresis Voltage	V_{t^+} - V_{t^-}	$0.1V_{DD}$	$0.4V_{DD}$	V
V_{OH}	Output High Voltage	$I_{OH} = -2mA$	$0.75V_{DD}$	1	V
V_{OL}	Output Low Voltage	I _{OL} = 2mA	1	$0.25V_{DD}$	V

Note(7): V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.

Note(8): For V_{t} + (V_{p}) and V_{t} - (V_{n}), V_{DD} refers to the receiving device. For V_{OH} and V_{OL} , V_{DD} refers to the sending device.

2.4.2 Optional Schmitt trigger operation – Wide range Wide range of optional schmitt trigger operation give in table 7.

Table 7 Wide range of optional schmitt trigger operation (9)(10)

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{DD}	Supply Voltage	_	0.8	1.3	V
$V_t + (V_p)$	Positive Going Threshold Voltage	V _{OUT} ≥V _{OH} (min)	$0.35V_{DD}$	$0.75V_{DD}$	V
V_{t} - (V_{n})	Negative Going Threshold Voltage	V _{OUT} ≤V _{OL} (max)	$0.25V_{DD}$	$0.65V_{DD}$	V
$V_h (V_t)$	Hysteresis Voltage	V_{t} + - V_{t} -	$0.1V_{DD}$	$0.5V_{DD}$	V
V _{OH}	Output High Voltage	$I_{OH} = -100 \mu A$	V _{DD} -0.1	_	V
V _{OL}	Output Low Voltage	$I_{OL}=100\mu A$	_	0.1	V

Note(9): V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.

Note(10): For V_t + (V_p) and V_t - (V_n), V_{DD} refers to the receiving device. For V_{OH} and V_{OL} , V_{DD} refers to the sending device.

3. Test conditions

- **3.1 Positive Going Threshold Voltage** [V_t + (V_p)] Input signal is raised from a grand level in the measurement circuit shown in Figure 1 , and the input voltage value of which output logic changed is determined as V_t + (V_p).
- 3.2 Negative Going Threshold Voltage[V_t (V_n)] Input signal is dropped from a power supply voltage level in the measurement circuit shown in Figure 1 , and the input voltage value of which output logic changed is determined as V_t (V_n).

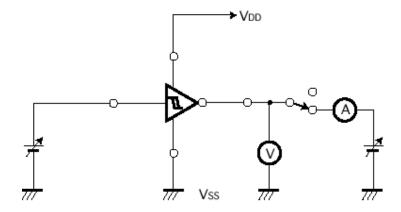


Figure 1 DC characteristic measurement circuit of Schmitt-trigger input

Explanation for 1.2V±0.1V (normal range) and 0.8V to 1.3V (wide range) Power supply voltage and interface standard for non-terminated digital integrated circuits

This explanation is not part of this JEITA standard. The discussion that follows provides descriptions of items defined or detailed in the standard body or in the Annex as well as other related topics.

1. Purpose of establishment This standard is enacted to accomplish a high speed and a low voltage operation of digital integrated circuits.

It defines power supply voltage ranges, DC interface parameters for a family of non-terminated digital circuits operating from a power supply of 1.2V and driving/driven by parts of the same family, or mixed families which comply with the input/output interface specifications.

Electronic Industries Association of Japan (EIAJ) and the Japan Electronic Development Association (JEIDA) have been merged effective on November 1, 2000, and become the Japan Electronics and Information Technology Industries Association (JEITA).

2. Review of discussion history JEDEC JC-16 (Low Voltage & High Speed Interface Sub-committee) in U.S.A, hereinafter called JEDEC, has committed to establish international standard of power supply voltage for digital circuits as a leader of the industry.

IC Low Voltage Operation Sub-committee, hereinafter called LVSC which was founded in 1992 as one of sub-committees of EIAJ and presently belongs to JEITA has cooperated with JEDEC and communicated mutually since its foundation.

For a long time, power supply voltage of digital circuits had been kept at 5V in general since 80's. However, in 90's, demand for low power supply voltage has surged to achieve low power consumption and high noise immunity of electric equipment, mainly in portable equipment (notebook PC, etc.) application, which requires longer battery life, and in high-performance equipment (WS, etc.) application, which requires faster response.

In 90's, a decade of deep sub-micron process technology (below 0.5µm process technology) has arrived. Low power supply voltage has become crucial issue to ensure reliability while offering high density and high speed.

Based on the aforementioned background, JEDEC started discussion on standard of low power supply voltage. First, in early 90's they started from the discussion on standard of 3.3V. As a result, 3.3V standard (JESD8-A) was established in June 1994 and consequently 2.5V standard (JESD8-5) in October 1995, 1.8V standard (JESD8-7) in February 1997 and 1.5V standard (JESD8-11) in October 2000.

LVSC also began the discussion on standard of low power supply voltage in April 1996, following JEDEC. It was encompassing penetration of 3.3V standard and delivery of much lower voltage standard from the second half of 90's. JEITA announced 3.3V standard (EIAJ ED-5001), 2.5V standard (EIAJ ED-5002) and 1.8V standard (EIAJ ED-5003) in May 1998 and the 1.5V standard (EIAJ ED-5004) in June 2000. Figures of these standards shall be identical to those of JEDEC in order to deliver unified symbols for above JEDEC standards.

Discussion on 1.2V standard was started by both JEDEC and LVSC in December 1999. LVSC submitted its proposed 1.2V standard to JEDEC in June 2000. Accordingly JEDEC approved 1.2V standard, which reflects the proposal of LVSC at the JEDEC meeting in September 2000. However, regarding to absolute maximum

EIAJ ED-5005A

ratings, JEDEC's proposal was adopted.

Based on the result of JEDEC meeting, JEITA's standard of 1.2V power supply voltage was finalized in February 2001.

This standard consists of normal range for regulated operation and wide range for battery operation, taking in consideration of 0.13µm class IC.

After standardizing the dc standard, discussion on Schmitt trigger input standard was started by JEITA / LVSC in February 2003. JEITA/LVSC submitted its proposed Schmitt trigger input standard to JEDEC in March 2004, for the first time. JEDEC's discussion on Schmitt trigger input standard was begun by this proposal. The task-group was organized by JEITA / LVSC and JEDEC at the JEDEC meeting in June 2004. It has decided that the proposal of Schmitt trigger standard to be added into existing dc standard. Finally, the proposal of Schmitt trigger input standard was approved at the JEDEC meeting in December 2004. Based on the result of JEDEC meeting, JEITA's revised standard of 1.2V power supply voltage was revised as ED-5005A in April 2006.

3. Members of discussion This standard has been discussed by the IC Low Voltage Operation Sub-committee which belongs to Group on Integrated Circuits of Technical Standardization Committee on Semiconductor Devices.

The members are shown as following.

< Technical Standardization Committee on Semiconductor Devices >

Chairman Hisao Kasuga NEC Electronics Corp.

< Group on Integrated Circuits >

Chairman Hisao Kasuga NEC Electronics Corp.

< IC Low Voltage Operation Sub-Committee >

Chairman	Haruyoshi Takaoka	Fujitsu Ltd.
Vice-chairman	Kohji Hosokawa	IBM Japan, Ltd.

Member Masahiro Kurimoto Oki Electric Industry Co., Ltd.

Hidemitsu Baba SANYO Electric Co.,Ltd.

Koji Inoue Sharp Corp.

Akira Nakada Seiko Epson Corp.

Mitsuo Soneta Sony Corp.

Masanori Kinugasa Toshiba Corp.

Takashi Akioka Renesas Corp.

Takefumi Yoshikawa Matsushita Electric Industrial Co.,Ltd.

Akitoshi Watanabe Rohm Co.,Ltd.

Guest Kazuo Yamaguchi TOSHIBA LSI System Support Corp.

Osamu Uno Fujitsu VLSI Ltd.

EIAJ ED-5005A

Secretariat Hideki Sato JEITA

Koji Kitada JEITA

EIAJ ED-5005A

Revised April, 2006

Published by Technical Standardization Center of Japan Electronics & Information Technology Industries Association

11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan

TEL+81-3-3518-6434 FAX +81-3-3295-8727