

JEITA

Standard of Japan Electronics and Information Technology Industries Association

ED-5001A

**3.3V±0.3V (normal range) and 2.7V to 3.6V (wide range)
power supply voltage and interface standard for
non-terminated digital integrated circuits**

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3.3V±0.3V (normal range) and 2.7V to 3.6V(wide range) power supply voltage and interface standard for non-terminated digital integrated circuit

Foreword To provide this standard of specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1. Scope This standard defines power supply voltage ranges, DC interface parameters for a family of nonterminated digital circuits operating from a power supply of 3.3V and driving/driven by parts of the same family, or mixed families which comply with the input/output interface specifications.

The specifications in this standard represent a minimum set or "base line" set of interfaces for LVTTTL-compatible and LVCMOS-compatible circuits.

2. Standard specifications All voltages listed are referenced to ground except where noted.

2.1 Absolute maximum continuous ratings Absolute maximum continuous ratings give in table 1.

Table 1 Absolute maximum continuous ratings ⁽¹⁾

Parameter	Symbol	Test condition	Rating	Unit
Power supply voltage	V _{DD}	–	–0.5 ~ 4.6	V
DC input voltage	V _{IN}	excluding I/O pins	–0.5 ~ V _{DD} +0.5(≤4.6 max)	V
DC output voltage	V _{OUT}	including I/O pins	–0.5 ~ V _{DD} +0.5(≤4.6 max)	V
DC input current	I _{IN}	V _{IN} < 0V or V _{IN} > V _{DD}	±20	mA
DC output current	I _{OUT}	V _{OUT} < 0V or V _{OUT} > V _{DD}	±20	mA
Storage temperature range	T _{STG}	–	⁽²⁾	°C

Note⁽¹⁾: Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum conditions is not implied, if it is beyond recommended operating conditions.

Note⁽²⁾: Specified by manufacturer for various purposes, respectively.

2.2 Recommended operating conditions Recommended operating conditions give in table 2.

Table 2 Recommended operating conditions

Parameter	Symbol	Normal range (3.3V nominal)	Wide range (3V nominal)	Unit
Power supply voltage	V _{DD}	3.0 ~ 3.6	2.7 ~ 3.6	V
Operating temperature range	T _a	⁽³⁾	⁽³⁾	°C

Note⁽³⁾: Specified by manufacturer for various purposes, respectively.

2.3 DC specifications All specifications in the following tables apply across the operating temperature range.

Table 3 LVTTTL & LVC MOS input specificationsWide range (3V nominal): $V_{DD}(\text{min}) = 2.7\text{V}$, $V_{DD}(\text{max}) = 3.6\text{V}$ Normal range (3.3V nominal): $V_{DD}(\text{min}) = 3.0\text{V}$, $V_{DD}(\text{max}) = 3.6\text{V}$

Parameter	Symbol	Test condition ⁽⁴⁾	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}(\text{min})$ or $V_{OUT} \leq V_{OL}(\text{max})$	2.0	$V_{DD} + 0.3$	V
Low-level input voltage	V_{IL}		-0.3	0.8	V
Input current	I_{IN}	$V_{IN} = 0\text{V}$ or $V_{IN} = V_{DD}$ ⁽⁵⁾	-	± 5	μA

Note⁽⁴⁾: For conditions shown as `min` or `max`, use the appropriate value shown in table 4 and table 5.**Note⁽⁵⁾:** Excluding common input/output terminals.**Table 4 LVTTTL output specifications**Normal range (3.3V nominal): $V_{DD}(\text{min}) = 3.0\text{V}$, $V_{DD}(\text{max}) = 3.6\text{V}$

Parameter	Symbol	Test condition	Min	Max	Unit
High-level input voltage	V_{OH}	$V_{DD} = \text{min}$, $I_{OH} = -2\text{mA}$	2.4	-	V
Low-level input voltage	V_{OL}	$V_{DD} = \text{min}$, $I_{OL} = 2\text{mA}$	-	0.4	V

Table 5 LVC MOS output specificationsWide range (3V nominal): $V_{DD}(\text{min}) = 2.7\text{V}$, $V_{DD}(\text{max}) = 3.6\text{V}$ Normal range (3.3V nominal): $V_{DD}(\text{min}) = 3.0\text{V}$, $V_{DD}(\text{max}) = 3.6\text{V}$

Parameter	Symbol	Test condition	Min	Max	Unit
High-level input voltage	V_{OH}	$V_{DD} = \text{min}$, $I_{OH} = -100\mu\text{A}$	$V_{DD} - 0.2$	-	V
Low-level input voltage	V_{OL}	$V_{DD} = \text{min}$, $I_{OL} = 100\mu\text{A}$	-	0.2	V

2.4 Optional DC electrical characteristics for Schmitt trigger operation All specifications in the following tables apply across the operating temperature range.

2.4.1 Optional Schmitt trigger operation – 3.3V Normal range 3.3V Normal range of optional schmitt trigger operation give in table 6.

Table 6 3.3V Normal range ⁽⁶⁾⁽⁷⁾

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{DD}	Supply Voltage	-	3.0	3.6	V
V_{t+} (V_p)	Positive Going Threshold Voltage	$V_{OUT} = V_{OH}(\text{min})$	0.9	2.1	V
V_{t-} (V_n)	Negative Going Threshold Voltage	$V_{OUT} = V_{OL}(\text{max})$	0.7	1.9	V
V_h (V_t)	Hysteresis Voltage	$V_{t+} - V_{t-}$	0.2	1.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu\text{A}$ $I_{OH} = -2\text{mA}$	$V_{DD} - 0.2$ 2.4	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu\text{A}$ $I_{OL} = 2\text{mA}$	-	0.2 0.4	V

Note⁽⁶⁾: V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.**Note⁽⁷⁾:** For V_{t+} (V_p) and V_{t-} (V_n), V_{DD} refers to the receiving device. For V_{OH} and V_{OL} , V_{DD} refers to

the sending device.

2.4.2 Optional Schmitt trigger operation – 3.3V Wide range 3.3V Wide range of optional schmitt trigger operation give in table 7.

Table 7 3.3V Wide range (8)(9)

Symbol	Parameter	Test Condition	Min	Max	Unit
V_{DD}	Supply Voltage	–	2.7	3.6	V
$V_{t+} (V_p)$	Positive Going Threshold Voltage	$V_{OUT} = V_{OH} (min)$	0.9	2.1	V
$V_{t-} (V_n)$	Negative Going Threshold Voltage	$V_{OUT} = V_{OL} (max)$	0.7	1.9	V
$V_h (V_t)$	Hysteresis Voltage	$V_{t+} - V_{t-}$	0.2	1.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\mu A$	$V_{DD} - 0.2$	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 100\mu A$	–	0.2	V

Note⁽⁸⁾: V_{DD} of the sending and receiving devices must track within 0.1 V to maintain adequate dc margins.

Note⁽⁹⁾: For $V_{t+} (V_p)$ and $V_{t-} (V_n)$, V_{DD} refers to the receiving device. For V_{OH} and V_{OL} , V_{DD} refers to the sending device.

3. Test conditions

3.1 Positive Going Threshold Voltage [$V_{t+} (V_p)$] Input signal is raised from a grand level in the measurement circuit shown in Figure 1 , and the input voltage value of which output logic changed is determined as $V_{t+} (V_p)$.

3.2 Negative Going Threshold Voltage[$V_{t-} (V_n)$] Input signal is dropped from a power supply voltage level in the measurement circuit shown in Figure 1 , and the input voltage value of which output logic changed is determined as $V_{t-} (V_p)$.

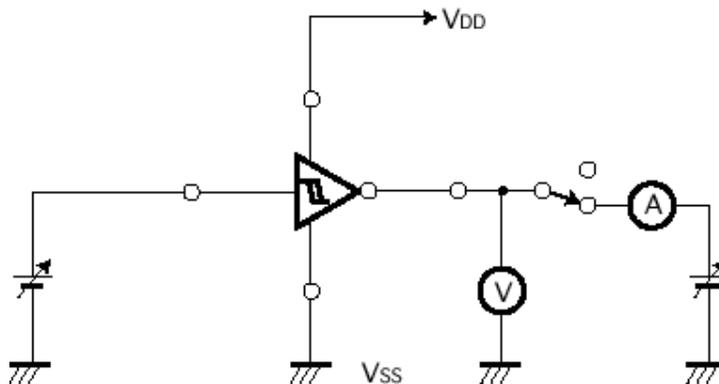


Figure 1 DC characteristic measurement circuit of Schmitt-trigger input

Explanation for 3.3V±0.3V (normal range) and 2.7V to 3.6V(wide range) power supply voltage and interface standard for non-terminated digital integrated circuit

This explanation is not part of this JEITA standard. The discussion that follows provides descriptions of items defined or detailed in the standard body or in the Annex as well as other related topics.

1. Purpose of establishment This standard is enacted to accomplish a high speed and a low voltage operation for digital integrated circuits.

This standard defines power supply voltage ranges, DC interface parameters for a family of nonterminated digital circuits operating from a power supply of 3.3V and driving/driven by parts of the same family, or mixed families which comply with the input/output interface specifications.

2. Review of discussion history JEDEC JC-16 (Low Voltage & High Speed Interface Sub-committee), called JEDEC after here, which belongs to EIA (Electronic Industries Association of U.S.A), enacted substantially the standard of power supply voltage for digital circuits in the world.

IC Low Voltage Operation Sub-committee which belongs to EIAJ(Electronic Industries Association of Japan) has been cooperation with JEDEC and communicated mutually, since it was founded in 1992.

A power supply voltage of digital circuits had been kept 5V,actually for a long time from 1980's. But, in 1990's, a requirement of low power supply voltage has become increasing to attain a low power consumption and a high noise immunity of electric equipments, in a main application of portable equipments (note PC, etc) which need a long battery operation and high performance equipments (WS, etc) which require a high speed.

In 1990's, also an age of deep sub-micron process technology (below 0.5μm process technology) has begun. Needs of low power supply voltage have become the most important issue to obtain a keeping of reliability and continuities of the trends of high density, high speed, together.

According to above back ground, discussion for standard of low power supply voltage, firstly 3.3V,have begun in JEDEC, from early of 1990's. 3.3V standard (JESD8-A) was enacted in June,1994, 2.5V standard (JESD8-5) was in October, 1995 and 1.8V standard (JESD8-7) was in February, 1997, respectively.

Especially, 3.3V JEDEC standard(JESD8-A) was required to maintain 5V TTL and 5V CMOS compatibility, because both 5V and 3.3V power supply voltages were used in a transition period from 5V to 3.3V when it was a first case of lower power supply voltage. To obtain a 5V compatibility, this standard defined a specifications of LVTTTL and LVCMOS.

Low Voltage Operation Sub-committee began the discussion for standard of low power supply voltage since April, 1996 in EIAJ, according to JEDEC's activities of power supply discussion, in anticipation of a real popularization of 3.3V power supply voltage from the half of 1990's and coming of next lower supply voltage than 3.3V.

EIAJ standard of 3.3V power supply voltage was established in May, 1998. This standard corresponds to that of JEDEC about specifications, because it has been already known and used widely in the world. But, this standard is amended from that of JEDEC about notation and sentence for accomplishing the unify of them among three JEDEC standards (3.3V, 2.5V, 1.8V).

After standardizing the dc standard, discussion on Schmitt trigger input standard was started by JEITA / LVSC in February 2003. JEITA/LVSC submitted its proposed Schmitt trigger input standard to JEDEC in March 2004, for the first time. JEDEC's discussion on Schmitt trigger input standard was begun by this proposal. The task-group was organized by JEITA / LVSC and JEDEC at the JEDEC meeting in June 2004. It has decided that the proposal of Schmitt trigger standard to be added into existing dc standard. Finally, the proposal of Schmitt trigger input standard was approved at the JEDEC meeting in December 2004. Based on the result of JEDEC meeting, JEITA's revised standard of 3.3V power supply voltage was revised as ED-5001A in April 2006.

3. Members of discussion This standard has been discussed by the IC Low Voltage Operation Sub-committee which belongs to Group on Integrated Circuits of Technical Standardization Committee on Semiconductor Devices.

The members are shown as following.

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